DATASHEET

UJT060A0X43-SRPZ: Non-Isolated Modules

7.5 to 14.4V_{DC} input; 0.5 to 2V_{DC} output; 60A output current

RoHS Compliant

The UJT060A0X43-SRPZ Digital MicroDLynx II™ modules are non-isolated DC-DC converters that can deliver up to 60A of output current. The modules operate over a 7.5 to 14.4VDC input range and provide an adjustable, precisely regulated output voltage from 0.5 to 2VDC. Output voltage is programmable via an external resistor divider or PMBus command. Features include the PMBus digital protocol, remote On/Off, Power Good, overcurrent, overvoltage and overtemperature protection. It includes a real -time compensation loop for optimizing the dynamic response to match the load.

Applications

- High current voltage rails for ASICs/high-performance processors
- High-current FPGA power (e.g. Xilinx, Intel)
- High-performance ARM processor power
- Networking processors (e.g. Broadcom, Marvell, NXP)
- Artificial intelligence (AI) processors and applications
- Distributed power architectures
- Intermediate bus voltage applications
- Telecommunications equipment
- Servers and storage applications
- Networking equipment
- Industrial equipment
- Test and measurement equipment

Features

- Wide input voltage range: 7.5 to 14.4V_{DC}
- Digital output voltage programming 0.5 to 2V_{DC} via external resistor divider or PMBus™
- Delivers up to 60A output current
- Operation of up to 4 modules in parallel
- Charge mode controller provides fast transient response, reduced output capacitance and increased stability
- Tightly regulated output voltage
- Low output ripple and noise
- Fixed switching frequency with capability of an external synchronization
- Small Size: 20.32 x 11.43mm^2, height 12.95mm MAX
  0.800 x 0.450inch^2, height 0.510inch MAX
- Digital interface compliant to PMBus™ Rev.1.3 protocol
- Positive remote On/Off logic
- Tracking and output voltage sequencing
- Black-box fault recording
- Input and output OV/UV protection
- Cycle-by-cycle output OCP/UCP
- Over/under temperature protection
- Wide operating temperature range -40°C to 85°C
- UL* 62368-1, 2nd Ed. Recognized, and TUV (EN62368-1, 2nd Ed.) Licensed
- ISO** 9001 and ISO 14001 certified manufacturing facilities
- Compliant to RoHS II EU “Directive 2011/65/EU” and amended “Directive (EU) 2015/863”
- Compatible in a Pb-free or SnPb reflow environment
- Compliant to IPC-9592B (Nov. 2012), Category 2, Class: I,
- Compliant to REACH Directive (EC) No 1907/2006

Electrical Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Device	Min	Max	Unit
Input Voltage (Continuous)	V_{in}	-0.3	15	V
CLK, DATA, SMBALERT, SYNC, ON/OFF, PG, DDC, V5P, SEQ, VS+, VS-		-0.3	6	V
VSET/SA, V1P5, ISHARE		-0.3	3	V
Operating Ambient Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-55	125	°C

CAUTION: This power module is not internally fused. An input line fuse must always be used.

This power module can be used in a wide variety of applications, ranging from simple standalone operation to an integrated part of sophisticated power architecture. To preserve maximum flexibility, internal fusing is not included, however, to achieve maximum safety and system protection, always use an input line fuse. The safety agencies require a fuse with a maximum rating of 35A (see Safety Considerations section). Based on the information provided in this Data Sheet on inrush energy and maximum dc input current, the same type of fuse with a lower rating can be used. Refer to the fuse manufacturer's Data Sheet for further information.

Recommended Operating Conditions

Parameter	Symbol	Min	Nominal	Max	Unit
Input Voltage (continuous)	V_{in} $V_{in,nom}$	7.5	12	14.4	V
Output voltage	V_o	0.5	1.2	2.0	V
Output current (continuous), $V_o = V_{o,min}$ to $V_{o,max}$	I_{out}	0		60	A
CLK, DATA, SMBALERT, SYNC, ON/OFF, PG, DDC, V5P, SEQ, VS+, VS-				5.0	V

See footnotes on page 3

Electrical Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions.

Parameter	Condition	Symbol	Min	Typical	Max	Unit
Operating Input Voltage	All	V_{in}	7.5	12	14.4	Vdc
Maximum Input Current (V_{in}=7.5V to 14.4V, I_o=$I_{o,\,max}$)	All	$I_{in,\,max}$			18.5	Adc
Input No Load Current (V_{in} = 12V, I_o = 0, module enabled)	$V_{o,\,set}$ = 0.5Vdc	$I_{in,\,no\ load}$		80		mA
Input No Load Current (V_{in} = 12V, I_o = 0, module enabled)	$V_{o,\,set}$ = 2.0 Vdc	$I_{in,\,no\ load}$		100		mA
Input Stand-by Current (V_{in} = 12V, module disabled)	All	$I_{in,\,stand\text{-}by}$		25		mA
Inrush Transient	All	I^2t			1	A^2s
Input Reflected Ripple Current, peak-to-peak (5Hz to 20MHz, 1µH source impedance; V_{in} =7.5V to 14.4V, I_o= $I_{o,max}$; See Test Configurations)	All			40		$mA_{pk\text{-}pk}$
Input Ripple Rejection (120Hz)	All			-58		dB
Output Voltage Set-point accuracy over entire output range 0 to 85°C, V_o = over entire range -40 to 85°C, V_o = over entire range	All	$V_{o,\,set}$	-0.5 -0.7		+0.5 +0.7	$\%V_{o,\,set}$
Voltage Regulation[1] Line Regulation (V_{in}=$V_{in,\,min}$ to $V_{in,\,max}$)	All			0.15		$\%V_{o,\,set}$
Load Regulation (I_o = $I_{o,\,min}$ to $I_{o,\,max}$)	All			0.15		$\%V_{o,\,set}$

FOOTNOTES

*UL is a registered trademark of Underwriters Laboratories, Inc.

†CSA is a registered trademark of Canadian Standards Association.

‡VDE is a registered trademark of Verband Deutscher Elektrotechniker e..V.

** ISO is a registered trademark of the International Organization of Standard

The PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF)

[1] Worst case Line and load regulation data, all temperatures, from design verification testing as per IPC9592.

Electrical Specifications (continued)

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information. PMBus adjustable parameters show default setting.

Parameter	Device	Symbol	Min	Typical	Max	Unit
Adjustment Range (selected by an external resistor divider)	All	V_o	0.6		1.8	Vdc
PMBus Adjustable Output Voltage	All	V_o	0.5		2.0	Vdc
PMBus Output Voltage Adjustment Step Size	All			±0.05		$\%V_{o, set}$
Remote Sense Range	All				0.5	Vdc
Output Ripple and Noise on nominal output (V_{in} = 12V, V_o = $V_{o, min}$ to $V_{o, max}$ and I_o=$I_{o, min}$ to $I_{o, max}$ C_o = 4 x 0.1uF || 12 x 47uF || 2 x 330uF) Peak-to-Peak (5Hz to 20MHz bandwidth) RMS (5Hz to 20MHz bandwidth)	All			22 4.8		mV_{pk-pk} mV_{rms}
External Capacitance						
ESR ≥ 0.15 mΩ	All	C_o	330		560	µF
ESR ≥ 10 mΩ	All	C_o	660		15000	µF
Output Current (in source mode)	All	$I_{o,max}$			60	A_{dc}
Output Current (in sink mode)	All	$I_{o,max}$	-50			A_{dc}
Output Current Limit Inception (Hiccup Mode), see current measurement accuracy I_{ACC}	All	$I_{o, lim}$		73		A
Efficiency (V_{in}= 12Vdc, T_A=25°C, I_o=$I_{o, max}$, V_o= $V_{o, set}$)	$V_{o, set}$ = 0.6Vdc	η		82.0		%
	$V_{o, set}$ = 1.0Vdc	η		86.9		%
	$V_{o, set}$ = 1.2Vdc	η		88.2		%
	$V_{o, set}$ = 1.8Vdc	η		90.6		%
	$V_{o, set}$ = 2.0Vdc	η		91.2		%
Switching Frequency	All	f_{sw}		500		kHz
Frequency Synchronization						
Synchronization Frequency Range	All		450		550	%
High-Level Input Voltage	All	V_{IH}	2.0			V
Low-Level Input Voltage	All	V_{IL}			0.4	V
Minimum Pulse Width, SYNC	All	t_{SYNC}	200			ns
Maximum SYNC rise time	All	t_{SYNC_SH}			10	ns

General Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information. PMBus adjustable parameters show default setting.

Parameter	Device	Symbol	Min	Typical	Max	Unit
On/Off Signal Interface						
Logic High (Module ON)						
Input High Current	All	I_{IH}			1	µA
Input High Voltage	All	V_{IH}	2.1		5	V
Logic Low (Module OFF)						
Input Low Current	All	I_{IL}			1	µA
Input Low Voltage	All	V_{IL}	0		0.5	V
Turn-On Delay and Rise Times ($V_{in}=V_{in,nom}$, $I_o=I_{o,max}$, V_o to within ±1% of steady state)						
Case I: Input power is applied for at least one second and then the On/Off input is enabled (delay from instant at which Von/Off is enabled until Vo = 10% of Vo, set)	All	T_{delay}		1.5		msec
Case II: On/OFF is enabled and then in put power is applied (delay form instant at which V_{in} = $V_{in,min}$ until Vo = 10% of $V_{o,set}$	All	T_{delay}		15		msec
Output voltage Rise time Time for Vo to rise from 10% of $V_{o,set}$ to 90% of $V_{o,set}$	All	T_{rise}		4		msec
Output voltage overshoot (T_A = 25°C V_{IN}= $V_{IN,min}$ to $V_{IN,max}$, I_O = $I_{O,min}$ to $I_{O,max}$) With or without maximum external capacitance	All				3	$\%V_{O,set}$
Over Temperature Protection (See Thermal Considerations section)	All	T_{OT}		125		°C
PMBus Over Temperature Warning Threshold	All	T_{WARN}		110		°C
Tracking Accuracy ($V_{in,min}$ to $V_{in,max}$; $I_{o,min}$ to $I_{o,max}$; 0V < V_{SEQ} < Vo)						
Power-Up: 1V/ms	All	V_{SEQ} –Vo			100	mV
Power-Down: 1V/ms	All	V_{SEQ} –Vo			100	mV
Input Undervoltage Lockout						
Turn-on Threshold	All			6.9		Vdc
Turn-off Threshold	All			6.6		Vdc
Hysteresis	All			0.3		Vdc
PMBus Adjustable Input Under Voltage Lockout Thresholds	All		6.9		14	Vdc
Resolution of Adjustable Input Under Voltage Threshold			8			mVdc
PGOOD (Power Good)[1]						
Signal Interface Open Drain, $V_{supply} \leq$ 5VDC						
Overvoltage Threshold for PGOOD ON	All			108		$\%V_{o,set}$
Overvoltage Threshold for PGOOD OFF	All			110		$\%V_{o,set}$
Undervoltage Threshold for PGOOD ON	All			90		$\%V_{o,set}$
Undervoltage Threshold for PGOOD OFF	All			88		$\%V_{o,set}$
Pullup Resistance of PGOOD pin	All			10	5.1	kΩ
Sink current capability into PGOOD pin	All		-		5	mA
Calculated MTBF (I_o=0.8$I_{o,max}$ T_A=40°C) Telcordia Issue 3 Method 1 Case 3	All			60,158,012		Hours
Weight	All			8.5(0.3)		g(oz.)

[1] Default factory settings.

Feature Interface Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information.

Parameter	Conditions	Symbol	Min	Typical	Max	Unit
PMBus Signal Interface Characteristics						
Input High Voltage (CLK, DATA)		V_{IH}	2.1			V
Input Low Voltage (CLK, DATA)		V_{IL}			0.8	V
Input high level current (CLK, DATA)		I_{IH}	-1		1	µA
Input low level current (CLK, DATA)		I_{IL}	-1		1	µA
Output Low Voltage (CLK, DATA, SMBALERT#)	I_{OUT}=2mA	V_{OL}			0.5	V
Output high level open drain leakage current (DATA, SMBALERT#)	V_{OUT}=3.6V	I_{OH}	-0.1		0.1	µA
PMBus Operating frequency range	Slave Mode	F_{PMB}	10		1000	kHz
Data hold time	Receive Mode Transmit Mode	$t_{HD:DAT}$	0 300			ns
Data setup time		$t_{SU:DAT}$	250			ns
Measurement System Characteristics						
V_{IN} measurement range		$V_{IN(rng)}$	0		18	V
V_{IN} measurement accuracy[1]	FS=18V	$V_{IN,\ ACC}$	-2		+2	% FS
Output current measurement range		$I_{OUT(RNG)}$	0		75	A
Output current measurement accuracy -40 to 85°C[2] V_{in}= $V_{in,\ min}$ to $V_{in,\ max}$, V_o = $V_{o,\ min}$ to $V_{o,\ max}$ and I_o=$I_{o,\ min}$ to $I_{o,\ max}$	FL=60A	I_{ACC}		-4.0 +4.0		% of FL
Temperature measurement accuracy @12Vin, 0°C to 85°C		T_{ACC}		-2.0 +2.0		°C
V_{OUT} measurement range		$V_{OUT(rng)}$	0		2	V
V_{OUT} measurement accuracy		$V_{OUT,\ ACC}$	-2.0		+1.0	%

[1] The actual input voltage is typically 100mV higher than the reported READ_VIN value due to the internal low-pass filter.
[2] Typical output current measurement accuracy for default factory calibration (V_{IN}=12V, V_O=1.2V).

Characteristics Curves

Characteristic Curves of 0.6V Output

The following figures provide typical characteristics for the 60A Digital MicroDLynx II™ at 12Vin/0.6Vo 25°C.

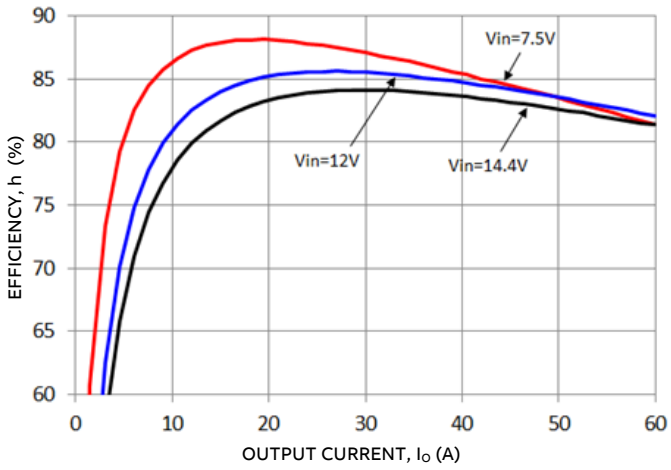

Figure 1. Converter Efficiency versus Output Current.

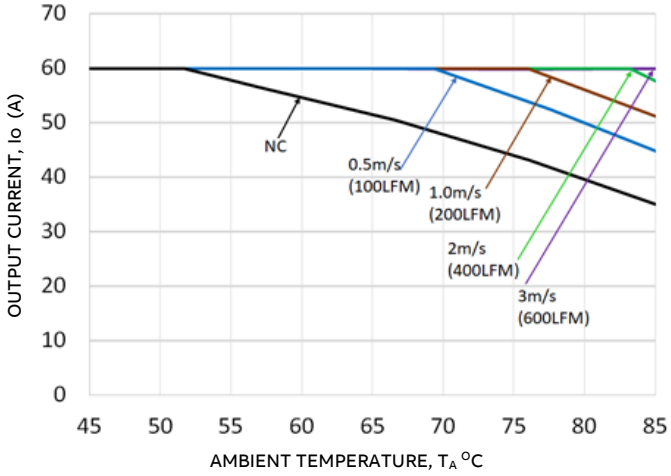

Figure 2. Derating Output Current versus Ambient Temperature and Airflow in preferred orientation.

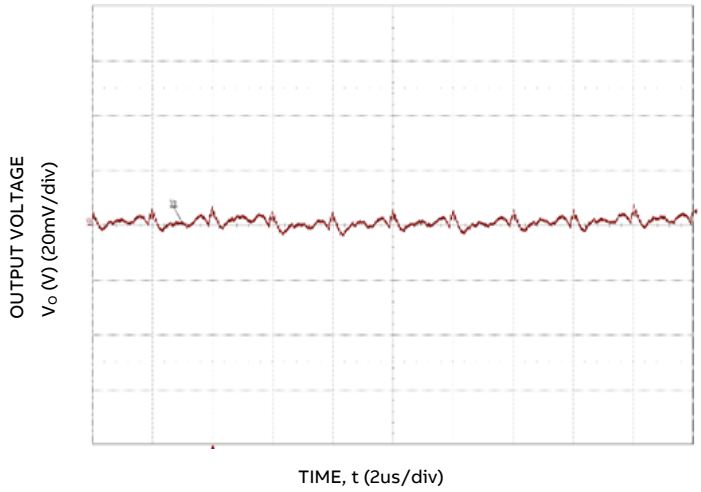

Figure 3. Typical output ripple and noise (C_o = 4x0.1µF + 12x47µF + 2x330µF polymer , V_{in} = 12V, I_o = $I_{o,max}$,).

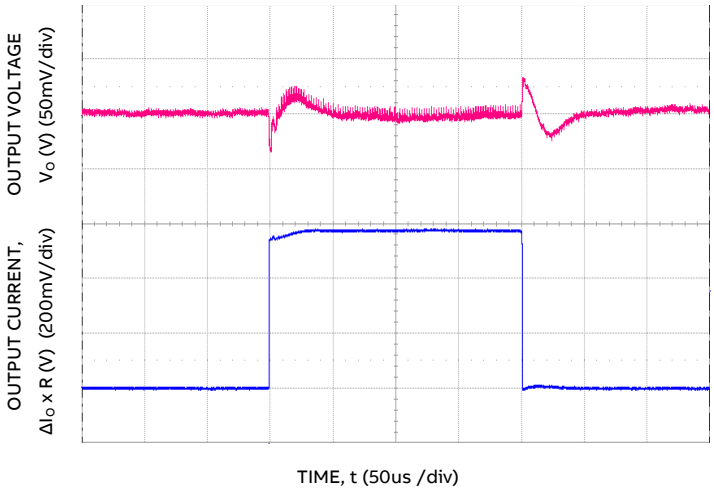

Figure 4. Transient Response to 100A/µs Dynamic Load Change from 25% to 75% at 12V_{in} (C_o = 4 x 0.1µF + 12 x 47µF + 12 x 1500µF, ASCR Gain = 256, ASCR Integrator = 128, ASCR Residual = 64). ΔIo=570mV/(0.2Ω/12)=34.2A

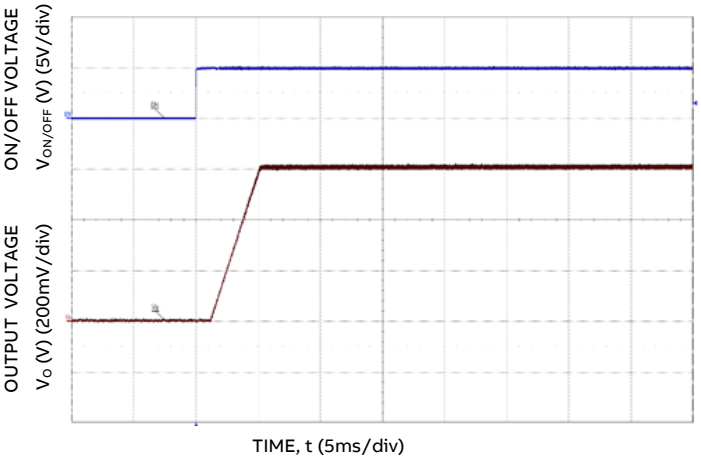

Figure 5. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

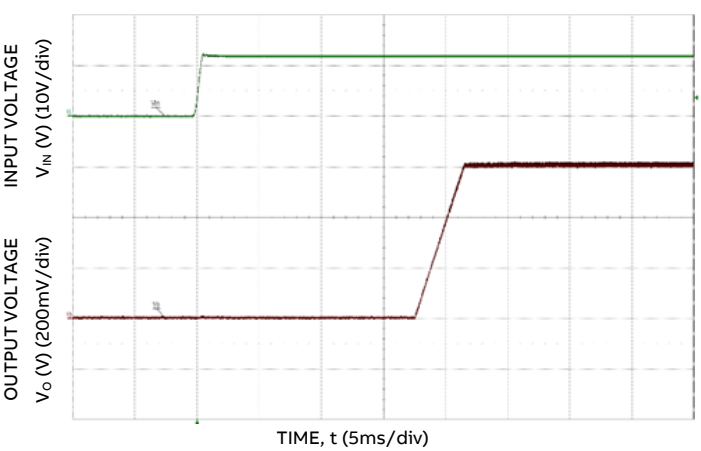

Figure 6. Typical Start-up Using Input Voltage (V_{in} = 12V, I_o = $I_{o,max}$).

Characteristics Curves

Characteristic Curves of 0.8V Output

The following figures provide typical characteristics for the 60A Digital MicroDLynx II™ at 12Vin/0.8Vo 25°C.

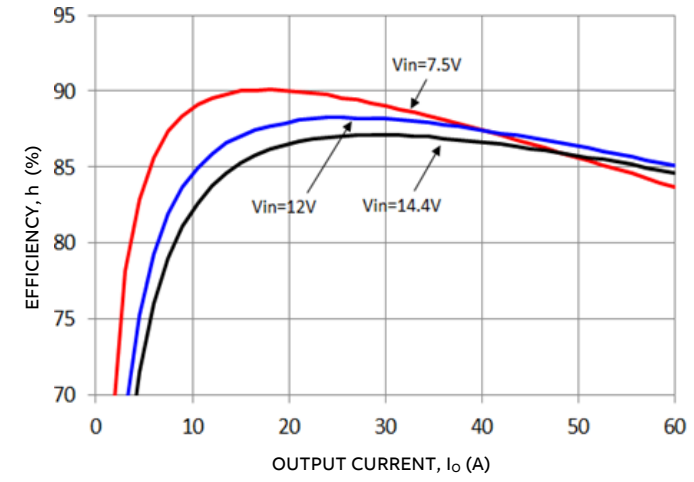

Figure 7. Converter Efficiency versus Output Current.

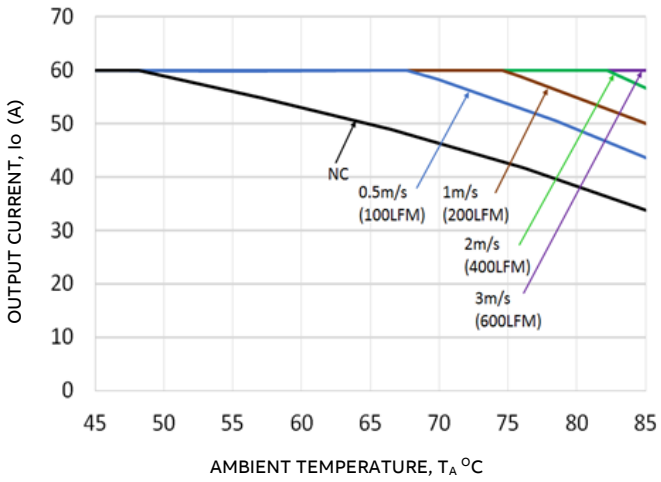

Figure 8. Derating Output Current versus Ambient Temperature and Airflow in preferred orientation.

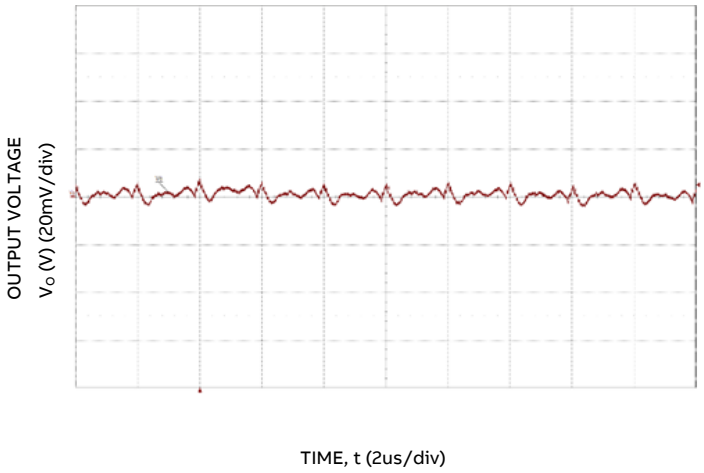

Figure 9. Typical output ripple and noise (C_o = 4x0.1µF + 12x47µF + 2x330µF polymer , V_{in} = 12V, I_o = $I_{o,max}$,).

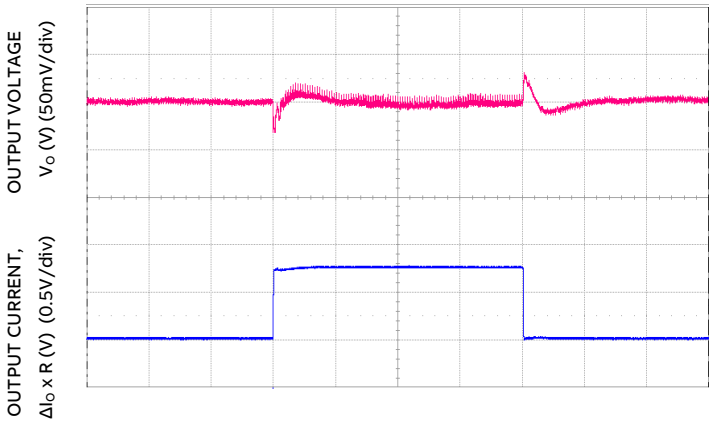

Figure 10. Transient Response to 100A/µs Dynamic Load Change from 25% to 75% at 12V_{in} (C_o = 4 x 0.1µF + 12 x 47µF + 12 x 1500µF, ASCR Gain = 256, ASCR Integrator = 128, ASCR Residual = 64). ΔIo=754mV/(0.2Ω/8)=30.2A

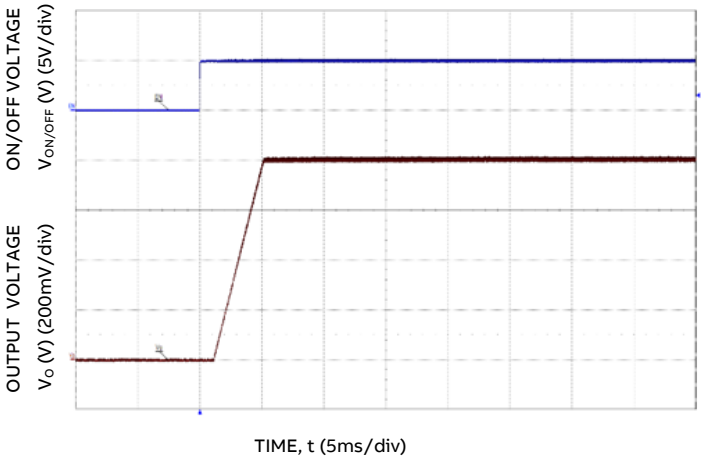

Figure 11. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

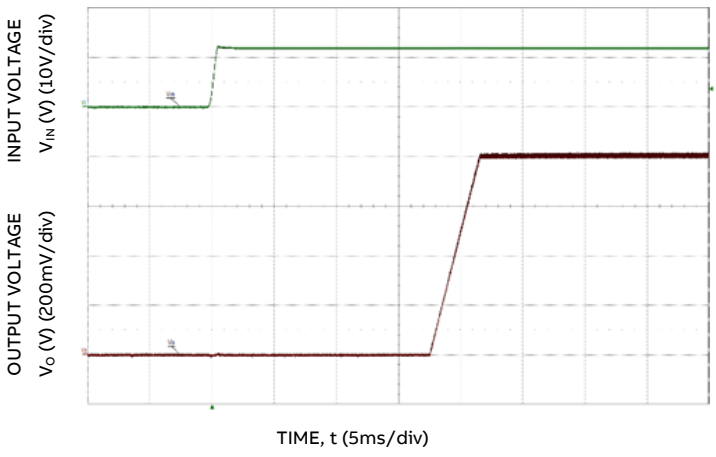

Figure 12. Typical Start-up Using Input Voltage (V_{in} = 12V, I_o = $I_{o,max}$).

Characteristics Curves

Characteristic Curves of 1.0V Output

The following figures provide typical characteristics for the 60A Digital MicroDLynx II™ at 12Vin/1.0Vo 25°C.

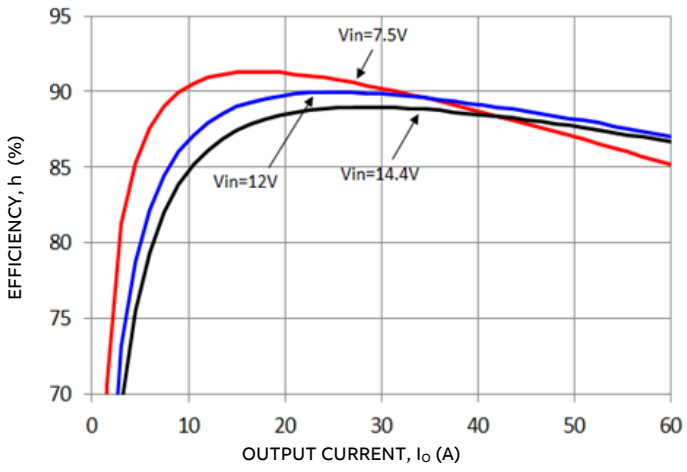

Figure 13. Converter Efficiency versus Output Current.

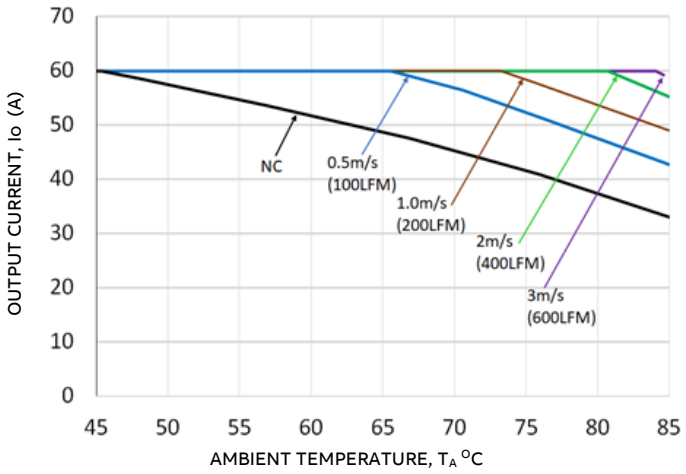

Figure 14. Derating Output Current versus Ambient Temperature and Airflow in preferred orientation.

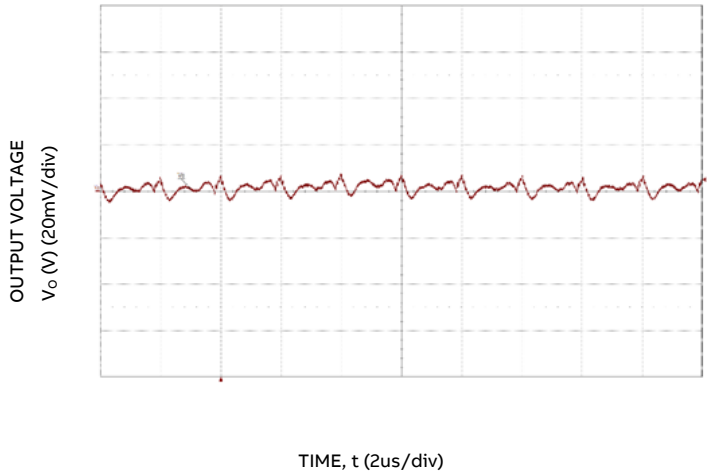

Figure 15. Typical output ripple and noise (C_o = 4x0.1µF + 12x47µF + 2x330µF polymer , V_{in} = 12V, I_o = $I_{o,max,}$).

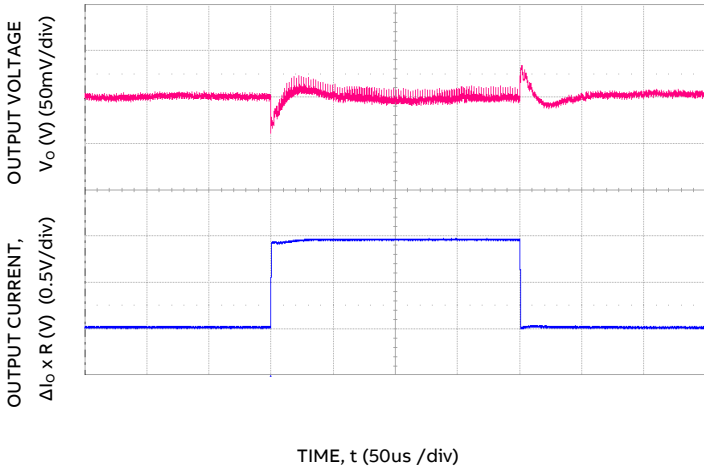

Figure 16. Transient Response to 100A/µs Dynamic Load Change from 25% to 75% at 12Vin (Co = 4 x 0.1µF + 12 x 47µF + 12 x 1500µF, ASCR Gain = 256, ASCR Integrator = 128, ASCR Residual = 64). ΔIo=950mV/(0.2Ω/7)=33.3A

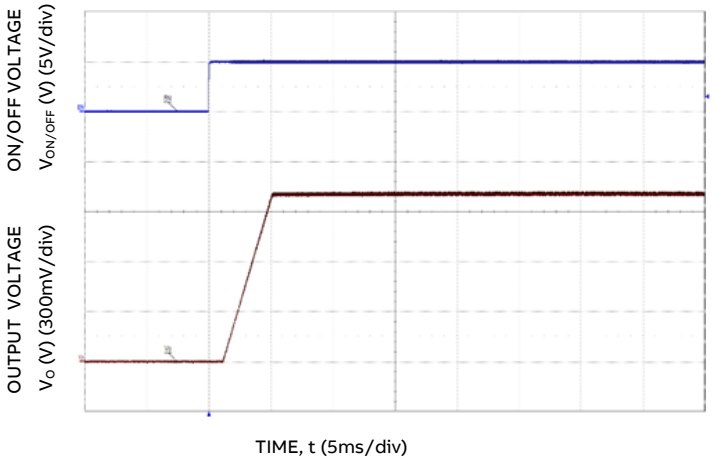

Figure 17. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

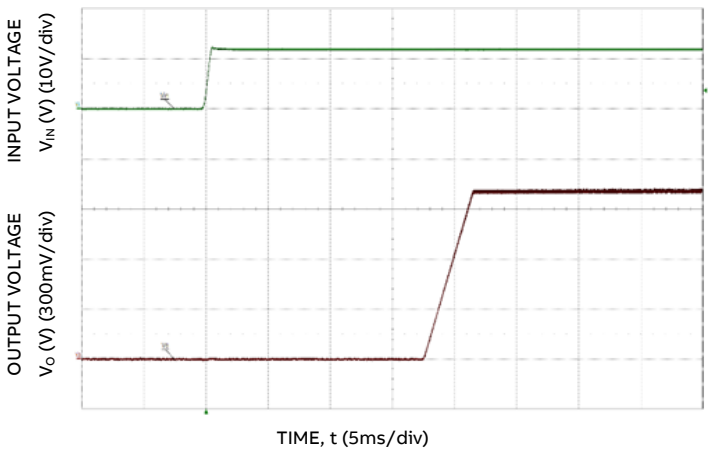

Figure 18. Typical Start-up Using Input Voltage (V_{in} = 12V, I_o = $I_{o,max}$).

Characteristics Curves

Characteristic Curves of 1.2V Output

The following figures provide typical characteristics for the 60A Digital MicroDLynx II™ at 12Vin/1.2Vo 25°C.

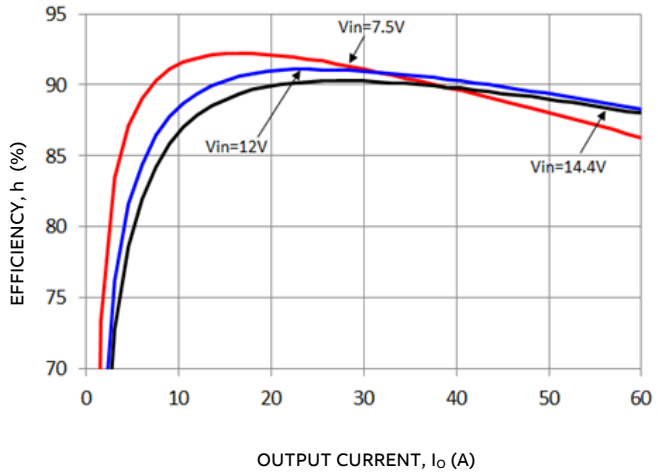

Figure 19. Converter Efficiency versus Output Current.

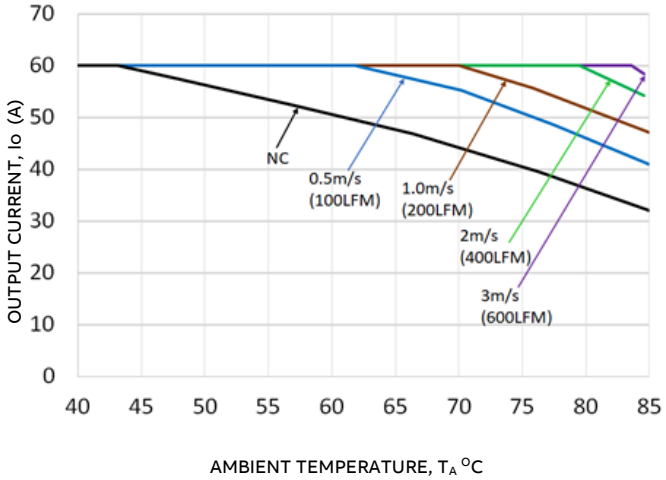

Figure 20. Derating Output Current versus Ambient Temperature and Airflow in preferred orientation.

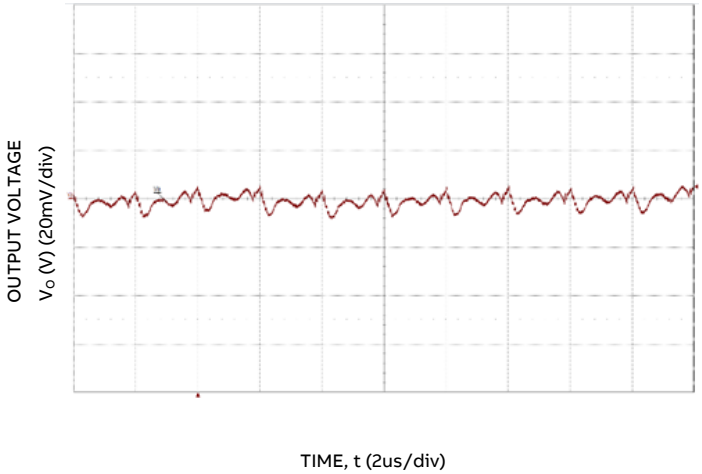

Figure 21. Typical output ripple and noise (C_o = 4x0.1µF + 12x47µF + 2x330µF polymer , V_{in} = 12V, I_o = $I_{o,max}$,).

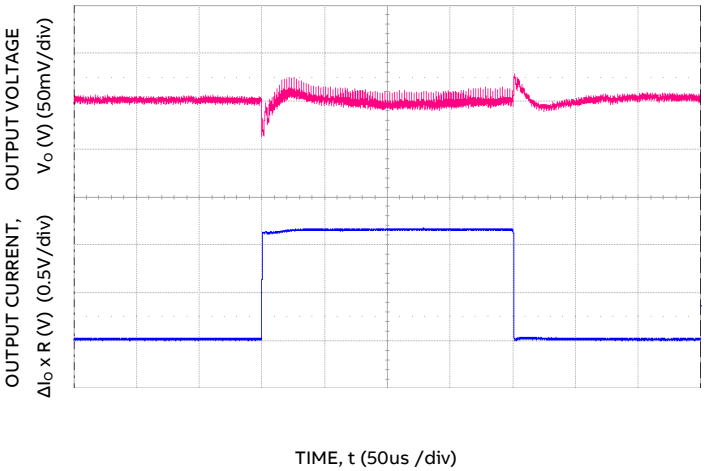

Figure 22. Transient Response to 100A/µs Dynamic Load Change from 25% to 75% at 12V_{in} (C_o = 4 x 0.1µF + 12 x 47µF + 12 x 1500µF, ASCR Gain = 256, ASCR Integrator = 128, ASCR Residual = 64). ΔIo=1.148V/(0.2Ω/6)=34.4A

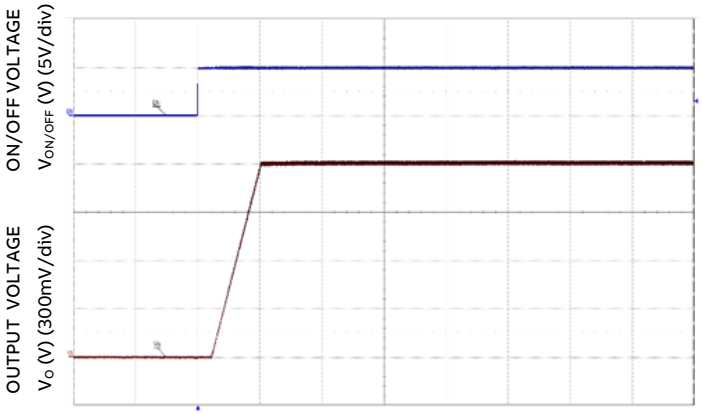

Figure 23. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

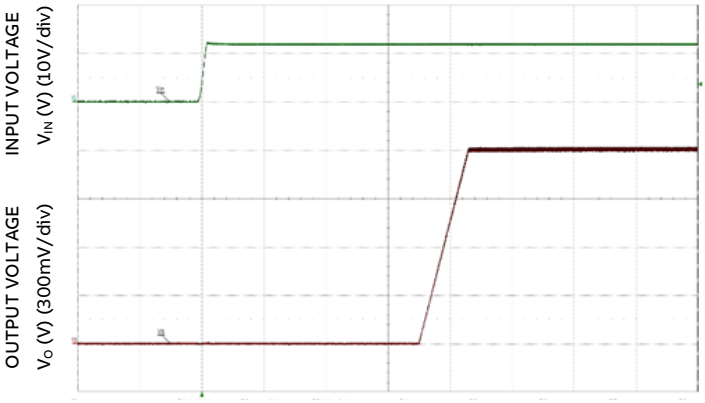

Figure 24. Typical Start-up Using Input Voltage (V_{in} = 12V, I_o = $I_{o,max}$).

Characteristics Curves

Characteristic Curves of 1.8V Output

The following figures provide typical characteristics for the 60A Digital MicroDLynx II™ at 12Vin/1.8Vo 25°C.

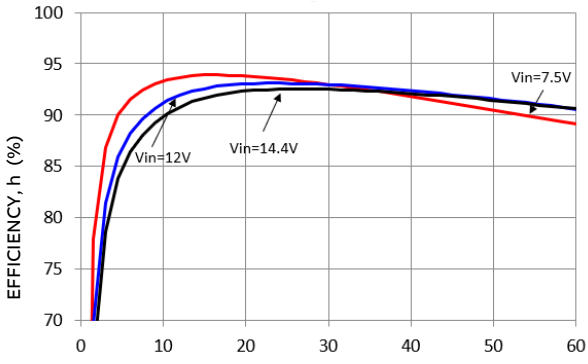

Figure 25. Converter Efficiency versus Output Current.

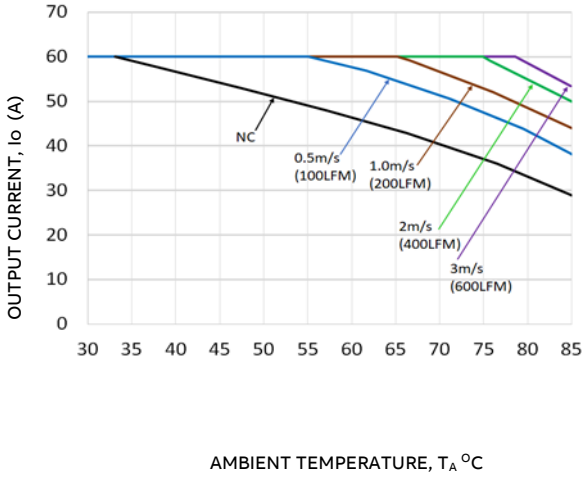

Figure 26. Derating Output Current versus Ambient Temperature and Airflow in preferred orientation.

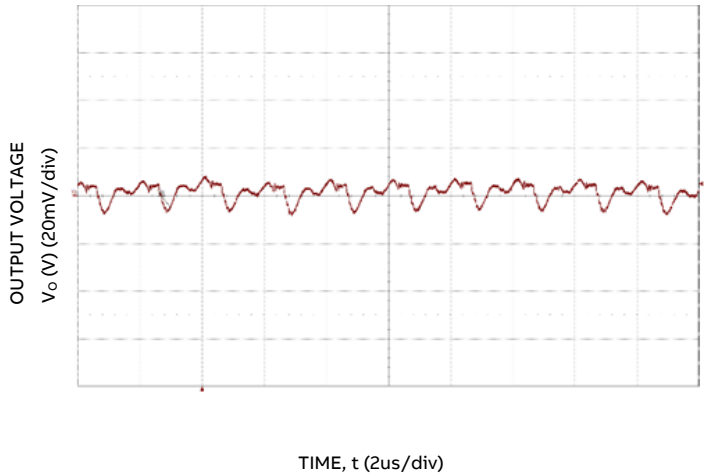

Figure 27. Typical output ripple and noise (C_o = 4x0.1µF + 12x47µF + 2x330µF polymer , V_{in} = 12V, I_o = $I_{o,max}$,).

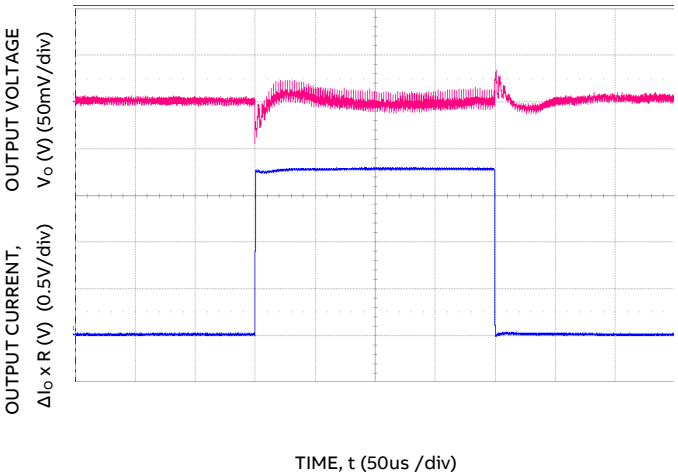

Figure 28. Transient Response to 100A/µs Dynamic Load Change from 25% to 75% at 12V_{in} (C_o = 4 x 0.1µF + 12 x 47µF + 12 x 1500µF, ASCR Gain = 256, ASCR Integrator = 128, ASCR Residual = 64). ΔIo=1.772V/(0.2Ω/4)=35.4A

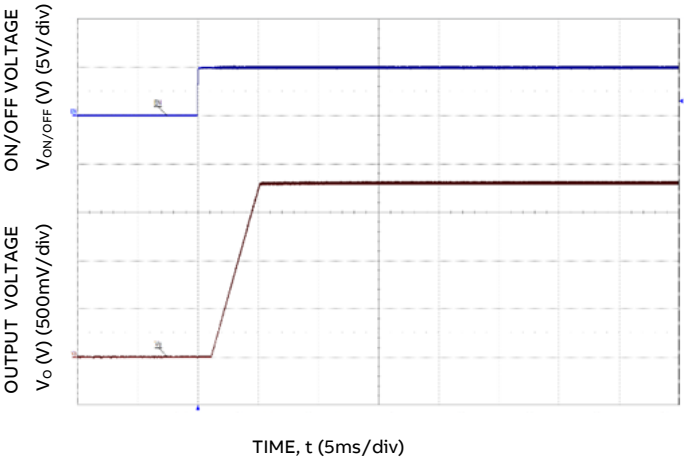

Figure 29. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

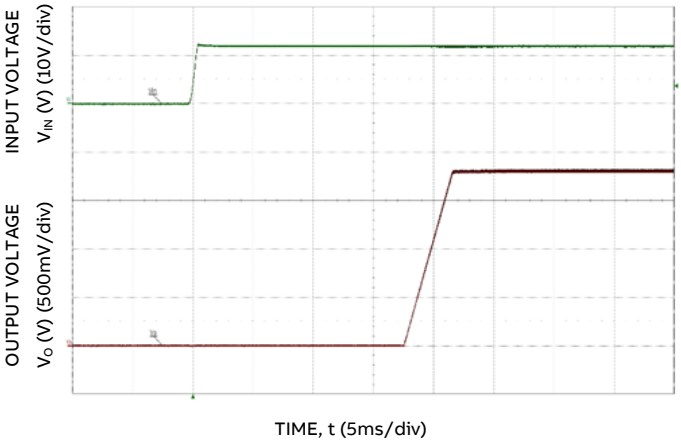

Figure 30. Typical Start-up Using Input Voltage (V_{in} = 12V, I_o = $I_{o,max}$).

Address and Output Voltage

Table I : Resistor Values for output voltages between 0.6V and 0.9V

Output Voltage		0.6V		0.7V		0.8V		0.9V	
ADDR	Hex Code	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)
16	10	32.4	3.16	93.1	9.09	158	15.8	232	22.6
17	11	25.5	3.32	71.5	9.31	124	16.2	178	23.2
18	12	20.5	3.4	59	9.76	100	16.5	147	24.3
19	13	17.4	3.48	49.9	10	84.5	16.9	124	24.9
20	14	15	3.57	43.2	10.5	73.2	17.8	107	25.5
21	15	13.3	3.74	38.3	10.7	64.9	18.2	93.1	26.1
22	16	11.8	3.83	34	11	57.6	18.7	84.5	27.4
23	17	11	4.12	30.9	11.5	52.3	19.6	75	28
24	18	9.76	4.12	28	11.8	47.5	20	69.8	29.4
25	19	9.09	4.32	26.7	12.7	44.2	21	64.9	30.9
26	1A	8.25	4.42	23.7	12.7	41.2	22.1	59	31.6
27	1B	7.68	4.64	22.1	13.3	37.4	22.6	54.9	33.2
28	1C	7.32	4.87	21	14	34.8	23.2	52.3	34.8
30	1E	6.49	5.36	18.2	15	31.6	26.1	45.3	37.4
31	1F	6.04	5.62	17.4	16.2	30.1	28	42.2	39.2
32	20	5.76	5.9	16.5	16.9	28	28.7	41.2	42.2
33	21	5.49	6.19	15.4	17.4	27.4	30.9	38.3	43.2
34	22	5.11	6.49	14.7	18.7	25.5	32.4	36.5	46.4
35	23	4.99	6.98	14.3	20	24.3	34	35.7	49.9
36	24	4.87	7.68	13.7	21.5	23.2	36.5	33.2	52.3
37	25	4.52	7.87	13	22.6	22.6	39.2	32.4	56.2
38	26	4.42	8.66	12.4	24.3	21.5	42.2	30.9	60.4
39	27	4.22	9.31	12.1	26.7	20.5	45.3	30.1	66.5
47	2F	4.12	10.2	11.5	28.7	20	49.9	28.7	71.5
48	30	4.02	11.5	11	31.6	19.1	54.9	27.4	78.7
49	31	3.92	12.7	11	35.7	19.1	61.9	26.7	86.6
50	32	3.65	14	10.5	40.2	17.8	68.1	26.1	100
51	33	3.57	16.2	10	45.2	17.4	78.7	25.5	115
52	34	3.48	18.7	10	53.6	16.9	93.1	24.3	133
53	35	3.32	22.1	9.53	63.4	16.2	110	23.7	158
54	36	3.24	28	9.31	80.6	16.2	133	23.2	196

Address and Output Voltage

Table II : Resistor Values for output voltages between 1.0V and 1.8V

Output Voltage		1.0V		1.2V		1.5V		1.8V	
ADDR	Hex Code	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)	Ra (kΩ)	Rb (kΩ)
16	10	309	30.1	392	38.3	475	47.5	576	57.6
17	11	237	30.9	301	39.2	374	48.7	453	59
18	12	196	32.4	249	41.2	301	49.9	365	60.4
19	13	165	33.2	210	42.2	261	52.3	309	61.9
20	14	143	34	182	44.2	221	53.6	267	64.9
21	15	127	35.7	158	44.2	196	54.9	237	66.5
22	16	113	36.5	143	46.4	178	57.6	215	69.8
23	17	102	38.3	130	48.7	158	59	191	71.5
24	18	93.1	39.2	118	49.9	143	60.4	174	73.2
25	19	86.6	41.2	107	51.1	133	63.4	165	78.7
26	1A	78.7	42.2	100	53.6	124	66.5	150	80.6
27	1B	73.2	44.2	93.1	56.2	113	68.1	140	84.5
28	1C	69.8	46.4	88.7	59	107	71.5	130	86.6
29	1D	64.9	48.7	82.5	61.9	100	75	121	90.9
30	1E	60.4	49.9	76.8	63.4	95.3	78.7	115	95.3
31	1F	57.6	53.6	73.2	68.1	90.9	84.5	110	102
32	20	54.9	56.2	69.8	71.5	84.5	86.6	100	102
33	21	52.3	59	66.5	75	82.5	93.1	100	113
34	22	49.9	63.4	63.4	80.6	76.8	97.6	93.1	118
35	23	47.5	66.5	60.4	84.5	75	105	88.7	124
36	24	45.3	71.5	57.6	90.9	69.8	110	84.5	133
37	25	43.2	75	54.9	95.3	69.8	121	84.5	147
38	26	42.2	82.5	53.6	105	64.9	127	78.7	154
39	27	40.2	88.7	51.1	113	63.4	140	75	165
47	2F	39.2	97.6	49.9	124	60.4	150	73.2	182
48	30	37.4	107	46.4	133	59	169	69.8	200
49	31	35.7	118	47.5	154	57.6	187	68.1	221
50	32	34.8	133	44.2	169	54.9	210	64.9	249
51	33	34	154	42.2	191	52.3	237	63.4	287
52	34	33.2	178	42.2	226	51.1	274	61.9	332
53	35	31.6	210	40.2	267	49.9	332	60.4	402
54	36	30.9	267	39.2	340	48.7	412	57.6	499

This page is left intentionally blank to mark the end of a section.

Design Consideration

Address and Output Voltage Selection

The address and output voltage are set by a 1% resistor divider from V1P5 pin to SIG_GND pin, the middle point of which is connected to the VSET pin. Varying combinations of resistor values will produce specific address and output voltage combinations. Refer to the Address and Output Voltage Table for possible combinations. Each UJT060A0X43-SRPZ module must have assigned a unique address. There are 32 available addresses and eight discrete output voltage settings from which to choose. The output voltage set point is not limited to the discrete values from the table and can be precisely adjusted by the VOUT_COMMAND 0x21. See parameter precedence below.

Please be advised that if the address resistors are omitted, resistor pair combination is wrong, or the connection to V1P5, VSET or SIG_GND pins is compromised, the controller will try to guess the intended address and output voltage settings, and therefore neither of them will be guaranteed. Compromised connections to module pins result in output voltage setting of 1.8V, unless VOUT_COMMAND value is stored into the non-volatile memory of the module!

Start-up Procedure

When the input voltage rises above the internal controller's Power-ON Reset (POR) level, approximately 4.5V, the module initialization begins. VSET and SYNC pins are read. These values along with the non-volatile FACTORY store are used to initialize the factory settings. Next, the contents of the DEFAULT store are read. Finally, the contents of the USER store are read. Upon completion of initialization routine, the PMBus communication is allowed and the controller begins to monitor the state of ON/OFF pin. Module initialization lasts approximately 15ms. The actual time depends on number of parameters stored into the non-volatile memory stores.

If a parameter is set by more than one mean, the value of the method with highest precedence wins. Assignment method precedence, from lowest to highest, is: pin-strap read, FACTORY store read, DEFAULT store read, USER store read and PMBus command write into volatile memory. The order of precedence could be changed by write protecting a parameter in the lower precedence store and enabling the password protection. See non-volatile memory management for details.

ON/OFF

The UJT060A0X43-SRPZ is a positive ON/OFF logic power module. The module is ON when the ON/OFF pin is at "logic high" state, and OFF when it is at "logic low" state. If negative ON/OFF logic is desirable, the inversion must be implemented on the customer side.

The module could be turned ON and OFF from an external enable signal or by the OPERATION 0x01 command. Desired behavior is set by ON_OFF_CONFIG 0x02 command. Use of external enable signal guarantee precise turn-on timing when several modules operate in parallel. For repeatable turn on delay, the enable signal should be asserted high after the controller initialization has been completed and the input voltage is above its undervoltage warning limit.
When enabling the device exclusively only via OPERATION command, it is recommended that the ON/OFF pin is tied to pin 15 (DGND).

The ON/OFF pin is edge triggered to achieve fast turn-on and turn-off times. As a result, minimum enable high and enable low pulse widths must be observed to ensure correct operation. Enable low and enable high times shorter than minimums shown below may result in the module not responding to the trailing edge of the pulse. For example, applying enable high pulse shorter than the minimum pulse width, will turn the module ON, but may not turn the module OFF until a valid enable high pulse is applied to the ON/OFF pin.

TEN_LOW > TOFF_DELAY + TOFF_FALL + 10.5ms

TEN_HIGH > TON_DELAY + TON_RISE + TPOWER_GOOD_DELAY + 5.5ms

The delay between the transition edge of enable signal or the receipt of an OPERATION command and the beginning of the change of the output voltage may be adjusted using TON_DELAY 0x60 and TOFF_DELAY 0x64 commands. When the Ton-delay time is set to 0ms, the device begins its ramp after the internal circuitry has initialized which takes approximately 100µs to complete.

Design Consideration (continued)

The desired rising and falling slopes of the output voltage can be set by TON_RISE 0x61 and TOFF_FALL 0x65 commands. The Ton-rise time can be set to values less than 125ms; however, the Ton-rise time should be set to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current. A lower Ton-rise time limit can be estimated using the formula:

TON_RISE (MIN) = COUT EXT x VOUT / (N x ILIMIT)

where COUT EXT is the total output capacitance, VOUT is the output voltage, N is the number of phases in parallel, and ILIMIT is the current limit setting for the module(s).

Power Good

The UJT060A0X43-SRPZ provides a power good signal, PG, that indicates the output voltage is within a specified tolerance of its target level and there are no fault conditions within the module. By default, the PG pin asserts if the output is within 10% of the target voltage. These limits and the configuration of the pin can be changed using POWER_GOOD_ON 0x5E and USER_CONFIG 0xD1 commands.

A PG delay period is defined as the time from when all the conditions within the module for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. The PG delay can be set using POWER_GOOD_DELAY 0xD4 command.

Pre-bias Startup

The UJT060A0X43-SRPZ supports pre-biased start-up operation in single mode and multi-phase operation mode. An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply is enabled. Certain applications require that the POL converter does not sink current during start up, if a pre-bias condition exists at the output. The module's control IC provides pre-bias protection by sampling the output voltage before initiating an output ramp. If a pre-bias voltage lower than the desired output voltage is present after the TON_DELAY 0x60 time the module starts switching with a duty cycle that matches the pre-bias voltage. This ensures that the ramp-up from the pre-bias voltage is monotonic. The output voltage is then ramped to the desired output voltage at the ramp rate set by the TON_RISE 0x61 command. The actual output voltage ramp duration vary with the pre-bias voltage level, however the output is always in regulation after a time interval equal to the sum of TON_DELAY 0x60 and TON_RISE 0x61.

If a pre-bias voltage higher than the target voltage exists after the preconfigured TON_DELAY 0x60 and TON_RISE 0x61 time have completed, the UJT060A0X43-SRPZ starts switching with a duty cycle that matches the pre-bias voltage, and then ramped down to the desired output voltage. This ensures that the ramp-down from the pre-bias voltage is monotonic. If a pre-bias voltage higher than the VOUT_OV_WARN_LIMIT 0x57 limit exists, the device does not initiate a turn-on sequence and stays off.

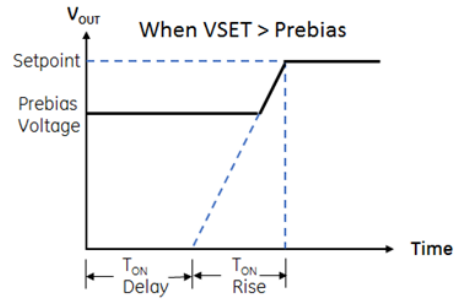

Figure 31a. Pre-bias Turn on

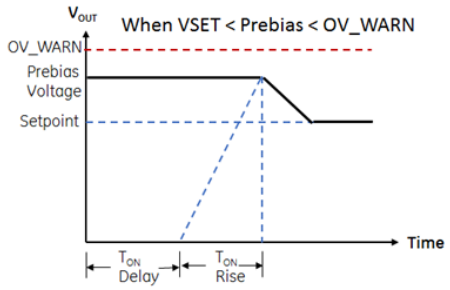

Figure 31b. Pre-bias Turn on

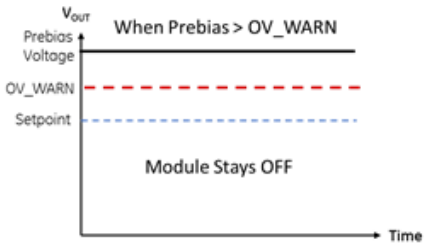

Figure 31c. Pre-bias Turn on

Voltage Tracking

The UJT060A0X43-SRPZ integrates a tracking scheme that allows its output to track a voltage that is applied to the SEQ pin with no external components required. The SEQ pin is an analog input. When tracking mode is enabled, the voltage applied to the SEQ pin acts as a reference for the module's output voltage regulation. The tracking functionality could be configured by TRACK_CONFIG 0xE1 command.

There are two tracking modes – coincident and ratiometric. In coincident mode the tracking is configured to ramp module's output voltage at the same rate as the voltage applied to the SEQ pin until it reaches module's programmed output voltage. Usually the programmed output voltage of a module that is tracking another output voltage is lower than final level of the tracking signal. In ratiometric mode the module's output voltage is 50% of the signal applied to the SEQ pin. Different ratios may be implemented using external resistor divider.

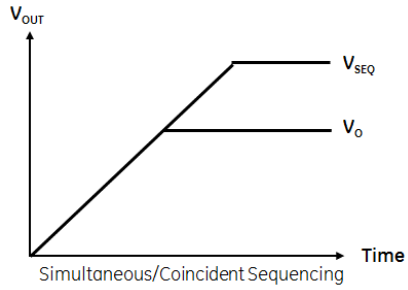

Figure 32a. Simultaneous Tracking

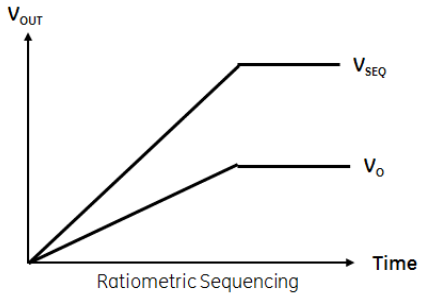

Figure 32b. Ratiometric Tracking

When tracking mode is enabled the output takes the characteristics of the tracked voltage. Sequencing events like enabling and disabling of the module as well as the soft-start settings TON_DELAY 0x60 and TON_RISE 0x61 are ignored. If the module's tracking target limit is chosen, the changes to VOUT_COMMAND 0x21 and output voltage margins are also ignored. POWER_GOOD_DELAY 0xD4 still applies.

The maximum tracking signal slew rate is 1V/ms. The device must be enabled at least 100µs before the tracking signal ramps up. If the voltage at the SEQ pin is greater than 0V prior to the module being enabled, the tracking voltage rises at the rate set by VOUT_TRANSITION_RATE 0x27 until it reaches the correct ratio of the tracked voltage. Until the output voltage completes the initial ramp, the input tracking signal should not ramp up. To properly track during the turn-off ramp down, the TOFF_DELAY 0x64 must be set be long enough to ensure that the module is turned off after the tracking input signal ramps down to the final value.

Output Sequencing

A group of UJT060A0X43-SRPZ modules can be configured to power up and down in predetermined sequences. This feature is especially useful when powering advanced processors, FPGAs, and ASICs. Each module, or group of modules operating in parallel, in the sequencing chain is informed for the module or the rail that need to power up before and the one that need to power up after. The ON/OFF pins of all modules in the sequencing group are tied together. When sequencing on, the first device to ramp up, called the "prequel", sends a message through the DDC bus to the next device, called the "sequel" when the prequel's PG signal is driven high. When sequencing off, the sequel sends a message to the prequel to begin the prequel's ramp down after the sequel has completed its own ramp down. To achieve sequenced turn-off all the modules in the sequencing group should be configured for soft turn-off using the ON_OFF_CONFIG 0x02 command. Sequencing can be configured by the SEQUENCE 0xE0 command.

Input Overvoltage and Undervoltage Protections

The input overvoltage and undervoltage protections prevent the UJT060A0X43-SRPZ from operating when the input is above or falls below preset thresholds. The customers are strongly advised not to increase the preset input overvoltage limit or decrease input undervoltage limit as it may result in compro-

mising product safety, violation of the module's absolute maximum and minimum ratings which will void the product warranty.

The input overvoltage and undervoltage protections could be adjusted by the following commands:
VIN_OV_FAULT_RESPONSE 0x56,
VIN_UV_FAULT_RESPONSE 0x5A,
VIN_OV_FAULT_LIMIT 0x55,
VIN_OV_WARN_LIMIT 0x57,
VIN_UV_WARN_LIMIT 0x58,
VIN_UV_FAULT_LIMIT 0x59.

See PMBus Commands for more details.

Output Overvoltage and Undervoltage Protections

The UJT060A0X43-SRPZ offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limit. The output voltage sensed through the VS+ and VS- pins is digitized and then compared to various programmable thresholds. The output undervoltage fault is masked during the module's soft-start output voltage ramp up, before the power good signal is asserted.

The UJT060A0X43-SRPZ overvoltage and undervoltage behavior ca be configured through the following commands: VOUT_OV_FAULT_RESPONSE 0x41,
VOUT_UV_FAULT_RESPON SE 0x45,
VOUT_OV_FAULT_LIMIT 0x40,
VOUT_OV_WARN_LIMIT 0x42,
VOUT_UV_WARN_LIMIT 0x43,
VOUT_UV_FAULT_LIMIT 0x44.

See PMBus Commands for more details.

Output Overcurrent and Undercurrent Protections

The output overcurrent and undercurrent protections prevent excessive forward current through the module and the load during abnormal operation and excessive reverse current through the module when, for example, the output is shorted to higher voltage rail. Overcurrent and undercurrent protections are cycle-by-cycle in nature. There are two types of fault limits: peak and valley limits IOUT_OC_FAULT_LIMIT 0x46 and IOUT_UC_FAULT_LIMIT 0x4B, and cycle-averaged limits IOUT_AVG_OC_FAULT_LIMIT 0xE7 and IOUT_AVG_UC_FAULT_ LIMIT 0xE8. **The customers are strongly advised not to increase the preset output overcurrent limits or decrease output undercurrent limits as it may result in compromising product safety, violation of the module's absolute maximum and minimum ratings which will void the product warranty.**

The output overcurrent and undercurrent warning limits and fault response could be adjusted by the following commands:
IOUT_OC_WARN_LIMIT 0x4A,
IOUT_UC_WARN_LIMIT 0x4B,
MFR_IOUT_OC_FAULT_RESPONSE 0xE5,
MFR_IOUT_UC_FAULT_RESPONSE 0xE6.

See PMBus Commands for more details.

There is another set of commands that affect the output current reading and indirectly overcurrent and undercurrent warning and protection levels. The appropriate values for these commands are saved into controller's non-volatile memory during manufacturing and the end user must not change them. These commands are: INDUCTOR 0xD6, ISENSE_CONFIG 0xD0, TEMPCO_CONFIG 0xDC, IOUT_CAL_GAIN 0x38 and IOUT_CAL_ OFFSET 0x39. Only in rare circumstances sophisticated users may slightly adjust the later two parameters to achieve superior output current accuracy for their specific application. During manufacturing, the output current calibration is performed at 12V input voltage and 1.2V output voltage at ambient temperature.

Overtemperature and Under-temperature Protections

The UJT060A0X43-SRPZ overtemperature protection ensures the temperature inside the module is below component's temperature maximum limit. The customers are strongly advised not to increase the preset overtemperature limit as it may result in compromising product safety, violation of the module's absolute maximum ratings which will void the product warranty. In addition to overtemperature protection, there is also under-temperature protection which although not essential for the product safety may be useful in some applications.

The overtemperature and under-temperature protections could be adjusted by the following commands:

OT_FAULT_RESPONSE 0x50,
UT_FAULT_RESPONSE 0x54,
OT_FAULT_LIMIT 0x4F,
OT_WARN_LIMIT 0x51,
UT_WARN_LIMIT 0x52,
UT_FAULT_LIMIT 0x53.

See PMBus Commands for more details.

Black-box faults logging

The UJT060A0X43-SRPZ black-box fault logging is a useful debugging tool. It provides valuable information for the operating condition when a fault has occurred. During normal operation the module is storing continuously parametric and status data into the RAM. When fault occurs this information is transferred into the flash. Eight of the most recently logged system snapshot remains in the memory for future reference.

The fault logging can be enable by SNAPSHOT_CONTROL 0xF3. The command is also used to specify when and how many snapshots will be taken, or which snapshot to be retrieved from memory. SNAPSHOT_FAULT_MASK 0xD7 command controls which faults will be ignored and will not triggered a snapshot event. SNAPSHOT 0xEA command with conjunction with SNAPSHOT_CONTROL 0xF3 command is used to read back 32-byte of parametric and status data. SNAPSHOT 0xEA command can also be used to log system data.

See PMBus Commands for more details.

Monitoring through SMBus

The UJT060A0X43-SRPZ controller can report a wide variety of system parameters through the SMBus interface. A fault condition in the module can be detected by monitoring the SMBALERT pin, which is asserted when any number of preconfigured fault conditions occur. The module can also be monitored continuously for any number of power conversion parameters. Some of the most useful monitoring commands are:
STATUS_BYTE 0x78,
STATUS_WORD 0x79,
STATUS_VOUT 0x7A,
STATUS_IOUT 0x7B,
STATUS_INPUT 0x7C,
STATUS_TEMPERATURE 0x7D,
READ_VIN 0x88,
READ_VOUT 0x8B,
READ_IOUT 0x8C,
READ_TEMPERATURE_1 0x8D.

See PMBus Commands for more details.

Input and Output Filtering

Because of its small size and compact design only a fraction of required input and output capacitance are placed inside the module. The additional external input capacitors must be placed adjacent to the input pins of the module. Combination of low ESR electrolytic and high-quality ceramic capacitors is recommended. To minimize the input-voltage ripple the ceramic capacitors must be placed closest to the input pins of the module. In a typical single-phase application, one should consider using at least one 470µF/16V electrolytic capacitor, ten 22µF X7R ceramic capacitors and two 0.1 µF X7R high frequency capacitors.

The amount of external output capacitance depends on the output transient and output ripple requirements. Part of the additional external output capacitors must be placed adjacent to the output pins of the module and the other part to the load. Combination of low ESR polymer and high-quality ceramic capacitors is recommended. To minimize the output voltage ripple part of the ceramic capacitors must be placed closer to the output of the module. To improve the load transient performance the other part of the ceramic capacitors must be placed closer to the load. In a typical single-phase application, one should consider using two 330µF/2.5V 18mΩ polymer capacitors, twelve 47µF X7R ceramic capacitors and four 0.1 µF X7R high frequency capacitors . Some demanding applications may require more output capacitance.

For high di/dt application, capacitor equivalent series inductance (ESL) becomes one of dominating factors of transient performance. ABB recommends user to use low ESL tantalum polymer as output bulk capacitor. ABB suggests user to use online Power Module Wizard or simulation tool to estimate the amount of capacitance required for the application, then choose right amount, size and type accordingly.

Control Loop Tuning

The heart of UJT060A0X43-SRPZ is a fully digital controller IC with innovative Charge Mode Control modulation scheme. By default, this control loop is stable for a wide range of output capacitance and loads, however, it may be further tuned to achieve higher performance under more specific application requirements. Since the control scheme is digital from end to end there is no dependence upon external compensation networks. This simplifies the design process by removing considerations such as temperature and process variation of passive components. Control parameters are set by ASCR_CONFIG 0xDF and ASCR_ADVANCED 0xD5 commands.

The ASCR gain parameter ASCR_CONFIG[15:0] represents the scaling of the error voltage as applied to setting the PWM pulse width. Increasing this parameter decreases the time the controller takes to respond to a transient event at the expense of being more susceptible to high frequency noise. This value is the dominant parameter for transient response tuning. We recommend increasing this parameter until the loop response time is sufficient for the application, but no more. Setting the ASCR gain parameter too high can lead to excessive output voltage ripple due to increased PWM jitter.

Integral gain ASCR_CONFIG[31:24] controls DC accuracy and the time taken to return to the output voltage set point following a transient event. Once ASCR gain is set appropriately, decrease integral gain while output voltage deviation is still acceptable.

Residual gain ASCR_CONFIG[23:16] is analogous to damping. The residual gain has the effect of removing or adding some fractional portion against the deviation of the PWM pulse width from steady state duty cycle in the next switch cycle created by the gain parameter. Increasing this parameter decreases output overshoot at the expense of prolonging the recovery to the output set point following a load transient. Its effect is delayed by one cycle relative to the gain effect and as such, it does not affect the peak voltage deviation during the transient, only the return to steady state.

In addition to the basic loop parameters, the controller incorporates a digital steady state gain reduction circuit to provide low jitter steady state operation while maintaining fast transient response. This circuit compares the error signal to the threshold set with ASCR_ADVANCED[11:0] over a period of time. If the error remains low, the controller begins dividing down the gain parameter according to the setting of ASCR_ADVANCED[13:12] to decrease the effect of high frequency noise on PWM pulse width. If the error exceeds the threshold in any cycle, the controller immediately reverts to the full gain setting to handle the transient. Once ASCR_CONFIG settings are chosen and output voltage ripple is acceptable in the application steady state conditions, increase the ASCR threshold setting until the gain reduction activates.

DDC Bus

The Digital Device Communication (DDC) bus provides communication channel between modules for features such as sequencing, fault spreading and current sharing. The DDC pin must be pulled-up to V5P before ON/OFF pin is set high, or to an external 3.3V or 5.0V supply which must be present before power-up. The DDC pull-up resistor must provide transition times shorter than, or equal to, 1µs. Generally, each module connected to the DDC bus presents approximately 12pF of capacitive loading. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that ensures a Logic Low, typically 0.8V. A 10kΩ resistor provides good performance on a DDC bus with fewer than 10 devices.

The UJT060A0X43-SRPZ modules can be configured to broadcast a fault event over the DDC bus to the other devices in the group. For details on DDC group ID assignment, addressing and configuration see DDC_CONFIG 0xD3 and DDC_GROUP 0xE2 commands.

Switching Frequency Setting

UJT060A0X43-SRPZ is optimized at 500kHz. In some application, user may choose to use higher switching frequency to achieve better output ripple voltage. Contact local ABB FAE for adjusting switching frequency.

Design Consideration (continued)

Synchronization

The UJT060A0X43-SRPZ's controller incorporates a precise 30MHz clock and Phase-Locked Loop (PLL) to clock the internal circuit. The switching frequency of the module is generated by dividing the internal clock by the closest integer number of times the value of switching frequency setting. The module is optimized to operate at 500kHz. When using the internal oscillator, the SYNC pin of one module can be configured as a clock source for other modules to accomplish phase spreading or phase interleaving.

The internal PLL circuit can also be synchronized to an external clock source connected to the SYNC pin. When the SYNC pin is configured as an input pin, the incoming clock signal must be in the range of ±10% of nominal switching frequency, must be present and stable within 50ms after POR and when the enable pin is asserted. The operation frequencies are not limited to discrete values as when using the internal clock.

In the event of a loss of the external clock signal, the PLL sets the External Switching Period Fault bit in the STATUS_MFR_SPECIFIC 0x80 and shut down the module. The module then changes the PLL input to its internal oscillator and commence switching at its programmed frequency upon re-enabling. To resume frequency synchronization, cycle POR with a valid clock signal applied at the SYNC pin or resend the USER_CONFIG 0xD1 command to "select external clock".

Phase Spreading

When multiple point-of-load converters share a common DC input supply, setting each converter to start its switching cycle at a different point in time can dramatically reduce the total peak and RMS input current and therefore improve system efficiency and reduce the input capacitance requirements. To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset can be configured using the INTERLEAVE 0x37 command.

Non-volatile Memory (NVM) Management

The UJT060A0X43-SRPZ has internal non-volatile memory where module's configurations are stored. There are three internal memory storage units: the USER store, the DEFAULT store and the FACTORY store. The USER store provides the end-user with ability to modify certain module settings while still protecting him, or her, from mistakes that may lead to a system level fault. The DEFAULT store provides a means to protect UJT060A0X43-SRPZ from damage by preventing the user from modifying certain values that are related to its physical construction, or safety and specification limits.

During the initialization process, the UJT060A0X43-SRPZ checks for stored values contained in its internal non-volatile memory. The parameters in USER store take priority over those in the DEFAULT store. If there are no values set in the USER, DEFAULT or FACTORY stores, the device uses the pin-strap setting value. Integrated security measures ensure that the user can only restore the module's configuration to a level that has been made available to them. For details regarding protection of the USER and DEFAULT stores, see the SECURITY_CONTROL 0xFA, PASSWORD 0xFB, WRITE_PROTECT 0xFD commands.

The ON/OFF pin must be driven low whenever a PMBus command that could potentially damage the application circuit is sent to the module. **It is always a good practice to turn the module OFF when saving configuration changes into the non-volatile memory.**

Parallel Operation and Active Current Sharing

Up to 4 UJT060A0X43-SRPZ modules can be paralleled together to form a high current rail. At steady-state operation the modules will share the current equally within a few percent, assuming output current sensing calibration is adequate. For most applications, factory performed calibration will be sufficient. In some application where the interconnecting impedances between modules are extremely low, in-system calibration may be necessary.

The UJT060A0X43-SRPZ employs "Master – Slave" active current sharing. The master in the current sharing rail continuously transmits its most recent output current reading through the SHARE bus, which the slave modules use as a reference for the purpose of the current balancing.

Only one master is allowed per current sharing rail. A simplified parallel operation schematic is shown in Figure 33. For several modules to form a current sharing group, the ON/OFF, SHARE, DDC and SYNC pins of one module must be connected to the same pin of all other modules. In addition, the output voltage sensing pins, VS+ and VS-, of each module in the group must be connected to the same output voltage regulation point. Often the ON/OFF bus would be configured for fault-spreading to ensure fast, 20µs typical delay time, fault response. In that scenario the ON/OFF bus would need a single 10kΩ pull-up resistor to V5P. When a module detects a fault condition, it will pull down the ON/OFF bus to disable the other modules in the current sharing group.

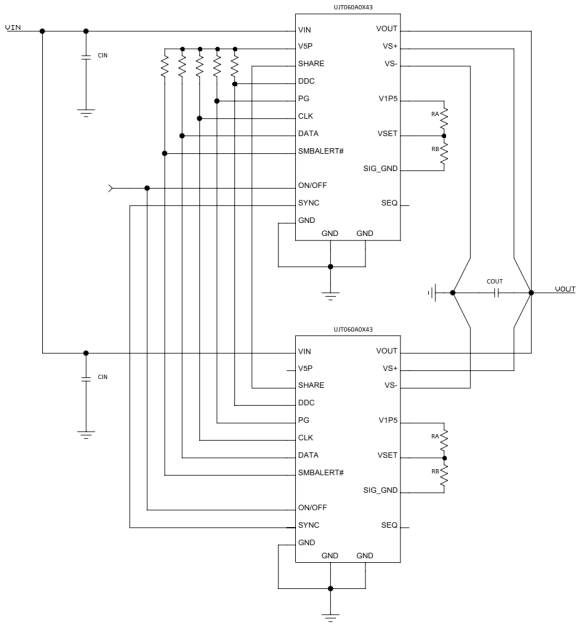

Figure 33. Simplified connection diagram for two devices in parallel

A current sharing rail may be configured using the following commands: USER_CONFIG 0xD1, DDC_CONFIG 0xD3 and DDC_GROUP 0xE2. The first step is to select a Rail ID number for the current sharing rail, establish the number of modules (phases) in the rail, and assign Phase IDs to each of the module. The Phase ID "0" identifies the master; all Phase ID settings in a rail must be sequential. All that could be configured by DDC_CONFIG 0xD3 command. Users must pay attention that every module in a multiphase rail share the same BROADCAST_VOUT_COMMAND and BROACAST_OPERATION DDC Group ID settings, which are distinct from DDC Rail IDs. DDC Group ID settings are configured with the DDC_GROUP 0xE2 command. By default, the phase interleaving of the modules in the current sharing rail is accomplished automatically. The controller of each module will choose its phase offset by the last four bits of its PMBus address. Therefore, it is a good practice, the addresses selected for the modules in a current sharing group to be sequential and to begin with the master of the group. The phase offset of the modules in the current sharing group could be altered by INTERLEAVE 0x37 command. For phase interleaving to work, all modules must be synchronized to an external clock, or to the clock of the master in the group. SYNC pin configuration could be set by USER_CONFIG 0xD1. The same command is used to configure the use of ON/OFF pin for fast fault-spreading.

Layout Considerations

The electrical and the thermal characterization of the UJT060A0X43-SRPZ module has been done on evaluation boards the layout of which is shown on Fig. 34. It demonstrates that very good noise immunity and thermal performance is possible to be achieved even with four-layer board.

Perhaps the most important rule to follow is the separation between signal ground and power ground. The module has a dedicated analog signal ground pin (10), a digital signal ground pin (15) and two power ground pins (2 and 3). All ground nets are internally connected. Pin 10 should be solely use as an analog return path for the external address resistor divider and for the tracking signal source. Pin 15 should be used as a return path for digital signals such as CLK, DATA, SMBALERT, ON/OFF, PG, DDC, ISHARE and SYNC.

To minimize the input rail noise coupling to the output of the module, use pin 2 for input rail return and pin 3 for output rail return. Note also that input and output ground planes are connected only on the top layer under the module's ground pins. System designer should always try to minimize the input and the output current loops by placing the input and output capacitors adjacent to the module's pins.

Route VS+ and VS– traces as a differential pair. Provide an analog ground plane under analog signal traces and digital ground plane under digital signal

Design Consideration (continued)

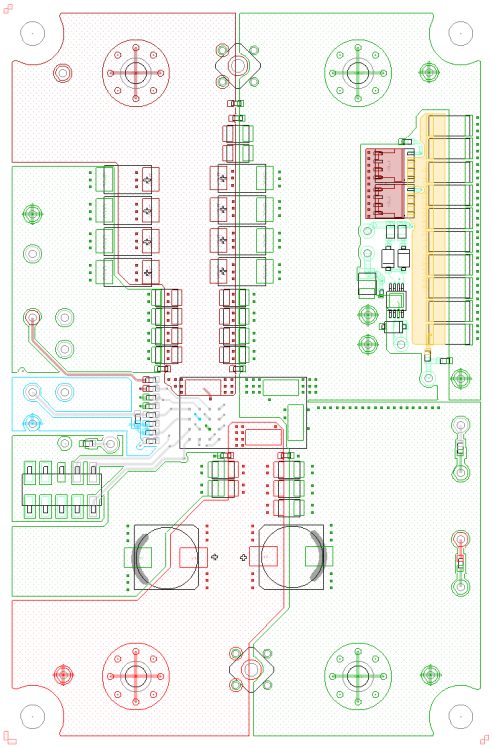

Figure 34a. Four-layer single module layout example. Top layer.

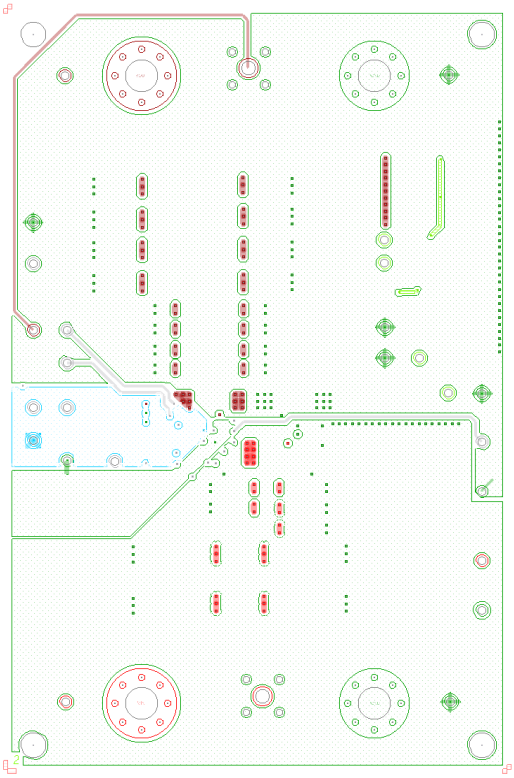

Figure 34b. Four-layer single module layout example. Layer two.

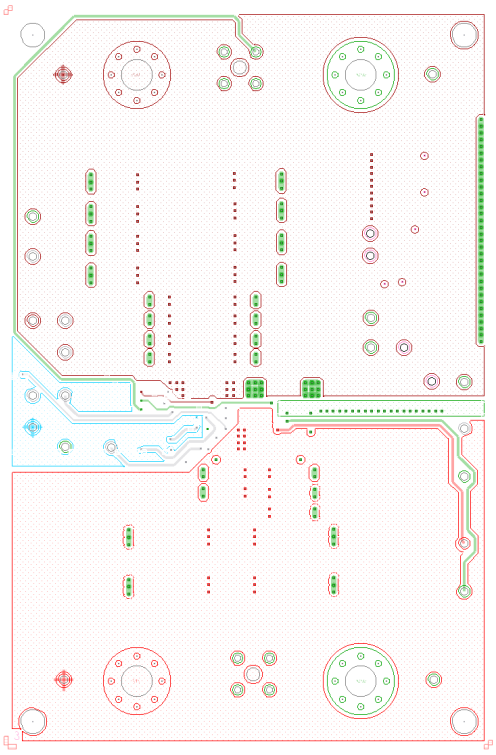

Figure 34c. Four-layer single module layout example. Layer three.

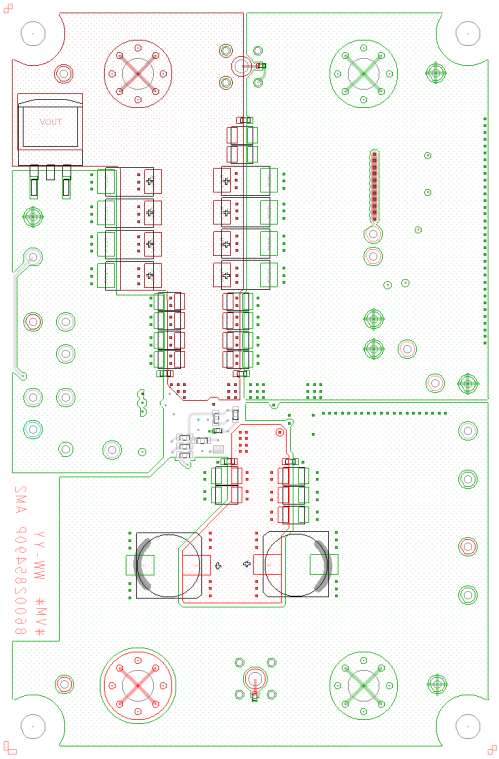

Figure 34d. Four-layer single module layout example. Bottom layer

traces. Route these traces as short as possible and away from noisy power planes.

Provide adequate number of through-hole via on the input and the output power plains near the module to facilitate thermal conduction to the system board and to distribute the input and the output currents between several layers. If forced air cooling is available, place the module near the source of cool air. Place high profile system components so they do not obstruct the airflow and achieve optimal thermal management.

Stencil Considerations

Solder volume is critical for reliable production process. Below table show the suggested stencil size for each pad type based on 7mil stencil thickness of customer board. See Fig. 38 Footprint dimensions .

PAD NO.	PAD SIZE (MIL)	STENCIL SIZE(MIL)
1-4	94 x 225 (X,Y)	89 x 220 (X,Y)
5-20	5-20	34 DIA

Safety Considerations

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e. UL* 62368-1, 2nd Ed. Recognized, and VDE (EN62368-1, 2nd Ed.) Licensed. For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV)/ES1, the input must meet SELV/ES1 requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV. The input to these units is to be provided with an external Littelfuse 456 series fast-acting fuse rated at 30A, 100Vdc in the ungrounded input.

Power Module Wizard

ABB offers a free, web based, easy to use tool that helps users simulate the loop performance of the UJT060A0X43-SRPZ. Go to http://abb.transim.com and sign up for a free account and use the module selector tool. The tool also offers downloadable Simplis/Simetrix, models that can be used to assess transient performance, module stability, etc. PLECS model is also available, consult local ABB FAE for details.

Digital Power Insight (DPI)

ABB offers a software tool that helps users evaluate and simulate the PMBus performance of the UJT060A modules without the need to write software. The software can be downloaded for free at http://powertalk.campaigns.abb.com/DigitalPowerInsight.html

An ABB USB to I2C adapter and associated cable set are required for proper functioning of the software suite. For first time users, we recommend using the ABB's DPI Evaluation Kit, which can be purchase from any of the leading distributors. Please ensure the ABB USB to I2C adapter being used/purchased is Version 2.2 or higher.

SMBus Interface and PMBus User Guidelines

The UJT060A0X43-SRPZ has a SMBus digital interface and can be used with any standard 2-wire SMBus host device. The module is compatible with SMBus version 2.0 and includes a SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the SMBus. The pull-up resistor can be tied to V5 or to an external 3.3V or 5V supply as long as this voltage is present before or during device power-up. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that ensures a Logic Low (typically 0.8V at the device monitoring point). Given the pull-up voltage of 5V and the pull-down current capability of the module (nominally 4mA), a 10kΩ resistor on each line provides good performance on an SMBus with fewer than 10 modules.

UJT060A0X43-SRPZ allows the user to adjust many parameters in order to optimize system performance. When configuring the module in a circuit, it should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION 0x01, ON_OFF_CONFIG 0x02, CLEAR_FAULTS 0x03, VOUT_COMMAND 0x21, VOUT_MARGIN_HIGH 0x25, and VOUT_MARGIN_LOW 0x26. While the module is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

When sending the STORE_DEFAULT_ALL 0x11, STORE_USER_ALL 0x15, RESTORE_DEFAULT_ALL 0x12, and RESTORE_USER_ALL 0x16 commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands. In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

The PMBus Host should respond to SALERT as follows: (1) Module pulls SALERT low. (2) PMBus host detects that SALERT is now low and performs transmission with Alert Response Address to find which module is pulling the SALERT low. (3) PMBus host talks to the module that has pulled SALERT low. The actions that the host performs are up to the system designer. If multiple modules are faulting and SALERT is low after performing the above steps, it requires transmission with the Alert Response Address repeatedly until all faults are cleared.

PMBus Data Format

Linear-11 (L11)
The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent real world decimal value (X). The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{N}$.
Linear-16 Unsigned (L16u)
The L16u data format uses a fixed exponent (hard-coded to N = -13d) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$.
Linear-16 Signed (L16s)
The L16s data format uses a fixed exponent (hard-coded to N = -13d) and a 16-bit two's complement mantissa (Y) to represent real world decimal value (X). The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$.
Bit Field (BIT)
A description of the Bit Field format is provided in each command details.
Custom (CUS)
A description of the Custom data format is provided in each command details. A combination of Bit Field and integer are common type of Custom data format.
ASCII (ASC)
A variable length string of text characters in the ASCII data format.

PMBus Command Summary

This section provides a summary of the UJT060A0X43 commands followed by their detailed description. The commands are outlined in the order of increasing command codes.

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	DATA UNITS	TRANS-FER TYPE	PROTECT ABLE	DEFAULT VAL-UE
OPERATION	0x01	1	bit field		R/W	No	0x00
ON_OFF_CONFIG	0x02	1	bit field		R/W	Yes	0x16
CLEAR_FAULTS	0x03	0			W	No	
STORE_DEFAULT_ALL	0x11	0			W	Yes	
RESTORE_DEFAULT_ALL	0x12	0			W	No	
STORE_USER_ALL	0x15	0			W	Yes	
RESTORE_USER_ALL	0x16	0			W	No	
CAPABILITY	0x19	1	bit field		R		0xD0
VOUT_MODE	0x20	1	mode + exp		R		0x13
VOUT_COMMAND	0x21	2	16-bit linear	V	R/W	Yes	VSET [1)]
VOUT_TRIM	0x22	2	16-bit linear	V	R/W	Yes	0.000V
VOUT_CAL_OFFSET	0x23	2	16-bit linear	V	R/W	Yes	0.000V
VOUT_MAX	0x24	2	16-bit linear	V	R/W	**Locked**	2.008V
VOUT_MARGIN_HIGH	0x25	2	16-bit linear	V	R/W	Yes	1.05 x VSET [1)]
VOUT_MARGIN_LOW	0x26	2	16-bit linear	V	R/W	Yes	0.95 x VSET [1)]
VOUT_TRANSITION_RATE	0x27	2	11-bit linear	V/ms	R/W	Yes	1V/ms
MAX_DUTY	0x32	2	11-bit linear	%	R/W	**Locked**	50%
FREQUENCY_SWITCH	0x33	2	11-bit linear	kHz	R/W	**Locked**	500kHz
POWER_MODE	0x34	1	bit field		R/W	Yes	0x00
INTERLEAVE	0x37	2	bit field		R/W	Yes	0x0000
IOUT_CAL_GAIN	0x38	2	11-bit linear	mΩ	R/W	**Locked**	vary
IOUT_CAL_OFFSET	0x39	2	11-bit linear	A	R/W	**Locked**	Vary
VOUT_OV_FAULT_LIMIT	0x40	2	16-bit linear	V	R/W	Yes	1.10 x VSET [1)]
VOUT_OV_FAULT_RESPONSE	0x41	1	bit field		R/W	Yes	0xB8
VOUT_OV_WARN_LIMIT	0x42	2	16-bit linear	V	R/W	Yes	1.08 x VSET [1)]
VOUT_UV_WARN_LIMIT	0x43	2	16-bit linear	V	R/W	Yes	0.88 x VSET [1)]
VOUT_UV_FAULT_LIMIT	0x44	2	16-bit linear	V	R/W	Yes	0.85 x VSET [1)]
VOUT_UV_FAULT_RESPONSE	0x45	1	bit field		R/W	Yes	0xB8
IOUT_OC_FAULT_LIMIT	0x46	2	11-bit linear	A	R/W	**Locked**	100.00A
IOUT_OC_WARN_LIMIT	0x4A	2	11-bit linear	A	R/W	Yes	65.00A
IOUT_UC_FAULT_LIMIT	0x4B	2	11-bit linear	A	R/W	**Locked**	-70.00A
OT_FAULT_LIMIT	0x4F	2	11-bit linear	°C	R/W	**Locked**	125°C

NOTES: 1) Output voltage setting according to VSET/SA pin-strap table.

PMBus Command Summary

This section provides a summary of the UJT060A0X43 commands followed by their detailed description. The commands are outlined in the order of increasing command codes.

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	DATA UNITS	TRANSFER TYPE	PROTECTABLE	DEFAULT VALUE
OT_FAULT_RESPONSE	0x50	1	bit field		R/W	Yes	0xB8
OT_WARN_LIMIT	0x51	2	11-bit linear	°C	R/W	Yes	110°C
UT_WARN_LIMIT	0x52	2	11-bit linear	°C	R/W	Yes	-45°C
UT_FAULT_LIMIT	0x53	2	11-bit linear	°C	R/W	Yes	-50°C
UT_FAULT_RESPONSE	0x54	1	bit field		R/W	Yes	0xB8
VIN_OV_FAULT_LIMIT	0x55	2	11-bit linear	V	R/W	**Locked**	16.0V
VIN_OV_FAULT_RESPONSE	0x56	1	bit field		R/W	Yes	0x80
VIN_OV_WARN_LIMIT	0x57	2	11-bit linear	V	R/W	Yes	14.5V
VIN_UV_WARN_LIMIT	0x58	2	11-bit linear	V	R/W	Yes	6.8V
VIN_UV_FAULT_LIMIT	0x59	2	11-bit linear	V	R/W	Yes	6.5V
VIN_UV_FAULT_RESPONSE	0x5A	1	bit field		R/W	Yes	0xB8
POWER_GOOD_ON	0x5E	2	11-bit linear	V	R/W	Yes	0.90 x VSET [1)]
TON_DELAY	0x60	2	11-bit linear	ms	R/W	Yes	0ms
TON_RISE	0x61	2	11-bit linear	ms	R/W	Yes	4ms
TOFF_DELAY	0x64	2	11-bit linear	ms	R/W	Yes	0ms
TOFF_FALL	0x65	2	11-bit linear	ms	R/W	Yes	2ms
STATUS_BYTE	0x78	1	bit field		R		
STATUS_WORD	0x79	2	bit field		R		
STATUS_VOUT	0x7A	1	bit field		R		
STATUS_IOUT	0x7B	1	bit field		R		
STATUS_INPUT	0x7C	1	bit field		R		
STATUS_TEMPERATURE	0x7D	1	bit field		R		
STATUS_CML	0x7E	1	bit field		R		
STATUS_MFR_SPECIFIC	0x80	1	bit field		R		
READ_VIN	0x88	2	11-bit linear	V	R		
READ_IIN	0x89	2	11-bit linear	A	R		
READ_VOUT	0x8B	2	11-bit linear	V	R		
READ_IOUT	0x8C	2	11-bit linear	A	R		
READ_TEMPERATURE_1	0x8D	2	11-bit linear	°C	R		
READ_DUTY_CYCLE	0x94	2	11-bit linear	%	R		
READ_FREQUENCY	0x95	2	11-bit linear	kHz	R		
READ_POUT	0x96	2	11-bit linear	W	R		
READ_PIN	0x97	2	11-bit linear	W	R		
PMBUS_REVISION	0x98	1	bit field		R		1.3

PMBus Command Summary

This section provides a summary of the UJT060A0X43 commands followed by their detailed description. The commands are outlined in the order of increasing command codes.

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	DATA UNITS	TRANSFER TYPE	PROTECTABLE	DEFAULT VALUE
IC_DEVICE_ID	0xAD	4	bit field		R		0x49A03100
IC_DEVICE_REV	0xAE	4	bit field		R		0x09000905
USER_DATA_00	0xB0	17	bit field		R/W	Yes	
USER_DATA_01	0xB1	17	bit field		R/W	Yes	
USER_DATA_02	0xB2	17	bit field		R/W	Yes	
ISENSE_CONFIG	0xD0	2	bit field		R/W	**Locked**	0x2201
USER_CONFIG	0xD1	2	bit field		R/W	Yes	0x0040
DDC_CONFIG	0xD3	2	bit field		R/W	Yes	0xXX00
POWER_GOOD_DELAY	0xD4	2	bit field	ms	R/W	Yes	1ms
ASCR_ADVANCED	0xD5	2	bit field		R/W	Yes	0x20FF
INDUCTOR	0xD6	2	11-bit linear	µH	R/W	**Locked**	0.185µH
SNAPSHOT_FAULT_MASK	0xD7	2	bit field		R	Yes	0x0000
OVUV_CONFIG	0xD8	1	bit field		R/W	Yes	0x02
MFR_SMBALERT_MASK	0xDB	7	bit field		R	Yes	0x00...00
TEMPCO_CONFIG	0xDC	1	bit field		R/W	**Locked**	0x2C
DEADTIME	0xDD	2	2x8-bit linear	ns	R/W	**Locked**	10ns/10ns
ASCR_CONFIG	0xDF	4	bit field				
SEQUENCE	0xE0	2	bit field		R/W	Yes	0x804000FF
TRACK_CONFIG	0xE1	1	bit field		R/W	Yes	0x0000
DDC_GROUP	0xE2	4	bit field		R/W	Yes	0x00
STORE_CONTROL	0xE3	1	bit field		R/W	Yes	
DEVICE_ID	0xE4	16	bit field		R		ISL68314-0-E0905
MFR_IOUT_OC_FAULT_RESPONSE	0xE5	1	bit field		R/W	Yes	0xB8
MFR_IOUT_UC_FAULT_RESPONSE	0xE6	1	bit field		R/W	Yes	0xBA
IOUT_AVG_OC_FAULT_LIMIT	0xE7	2	11-bit linear	A	R/W	**Locked**	75A
IOUT_AVG_UC_FAULT_LIMIT	0xE8	2	11-bit linear	A	R/W	**Locked**	-50A
SNAPSHOT	0xEA	32	bit field		R	Yes	
BLANK_PARAMS	0xEB	32	bit field		R/W	Yes	
STORE_DATA	0xF2	4	bit field		R/W	Yes	
SNAPSHOT_CONTROL	0xF3	2	bit field		R/W	Yes	0x0800
PINSTRAP_READ_STATUS	0xF5	5	bit field		R		
IIN_CAL_OFFSET	0xF6	2	11-bit linear	A	R/W	Yes	0.0A
SECURITY_CONTROL	0xFA	1	bit field		R/W	No	0x01
PASSWORD	0xFB	9	bit field		W	No	
WRITE_PROTECT	0xFD	32	bit field		R/W	Yes	

NOTES: 1) Output voltage setting according to VSET/SA pin-strap table.

Detailed Description of Supported PMBus Commands

Each command will have the following basic information.
Command Name (Code)
Definition
Data format
Factory default
Additional information may be provided if necessary.

OPERATION (0x01)

Definition: Changes output state of the module, sets V_{OUT} margins and margin's fault response .

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	N/A							
Bits	Purpose			Bit Value	Meaning			
7	Controls module output state			**0**	**Off (see ON_OFF_CONFIG)**			
				1	On (see ON_OFF_CONFIG)			
6	Controls the power down behavior.			**0**	**Device is immediately turned off. TOFF_DELAY and TOFF_FALL are ignored.**			
				1	Device is turned off observing TOFF_DELAY and TOFF_FALL			
5:4	Output Voltage			**00**	**VOUT is set by VOUT_COMMAND**			
				01	VOUT is set by VOUT_MARGIN_LOW			
				10	VOUT is set by VOUT_MARGIN_HIGH			
				11	Not used			
3:2	Margin Fault Response			**00**	**Not used**			
				01	Faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are ignored.			
				10	Faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are acted on			
				11	Not used			
1:0	Not used			00	Not used			

ON_OFF_CONFIG (0x02)

Definition: Configures the interpretation and coordination of the OPERATION command and the ON/OFF pin state .

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not used	Not used	Not used	pu	cmd	cpr	pol	cpa
Default Value	0	0	0	1	0	1	1	0
Bits	Purpose			Bit Value	Meaning			
7:5	Not Used			000	Not Used			
4	Coordinates the response to the OPERATION command and ON/OFF pin state .			0	Device is always on			
				1	**Device does not power up until commanded by the EN pin and OPERATION command (as programmed in Bits [3:0]).**			
3	Set the response to the OPERATION command .			**0**	0 Ignores on/off portion of the OPERATION command			
				1	Responds to on/off portion of the OPERATION command according to the setting of Bit 2			
2	Set the response to the ON/OFF pin state			0	Ignores ON/OFF pin (on/off controlled by the OPERATION command only)			
				1	Requires the ON/OFF pin to be asserted to start the module. May also require OPERATION command depending on Bit 4.			
1	Polarity of ENABLE pin			0	Not Used			
				1	**Active high only**			
0	ENABLE pin action when commanding the unit to turn off			**0**	**Use the configured ramp-down settings (“soft-off”)**			
				1	Turn off the output immediately			

CLEAR_FAULTS (0x03)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit reasserts immediately. This command does not restart a device if it has shut down, it only clears the faults.

STORE_DEFAULT_ALL (0x11)

Definition: Stores all current PMBus values from the operating memory into the nonvolatile DEFAULT store memory. To clear the DEFAULT store, perform a RESTORE_FACTORY then STORE_DEFAULT_ALL. To add to the DEFAULT store, perform a RESTORE_DEFAULT_ALL, write commands to be added, then STORE_DEFAULT_ALL. This command should not be used during device operation, the device is unresponsive for 100ms while storing values.

RESTORE_DEFAULT_ALL (0x12)

Definition: Restores PMBus settings from the nonvolatile DEFAULT store memory into the operating memory. These settings are loaded during at power-up if not superseded by settings in USER store. Security level is changed to Level 1 following this command. This command should not be used during device operation, the device is unresponsive for 100ms while storing values.

STORE_USER_ALL (0x15)

Definition: Stores all PMBus settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command should not be used during device operation; the device is unresponsive for 100ms while storing values.

RESTORE_USER_ALL (0x16)

Definition: Restores all PMBus settings from the USER store memory to the operating memory. Command performed at power-up. Do not use this command during device operation; the device is unresponsive for 100ms while restoring values.

CAPABILITY (0x19)

Definition: Reports some of the device's communications capabilities and limits.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	1	1	0	1	0	0	0	0

Bits	Purpose	Bit Value	Meaning
7	Packet Error Checking	0	Packet Error Checking not supported.
		1	**Packet Error Checking is supported.**
6:5	Maximum Bus Speed	**10**	**Maximum supported bus speed is 1MHz**
4	SMBALERT#	0	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol.
		1	**The device has a SMBALERT# pin and supports the SMBus Alert Response protocol.**
3	Numeric Format	**0**	**Numeric data is in LINEAR or DIRECT format.**
2	AVSBus Support	**0**	**AVSBus is not supported.**
1:0	Not Used	00	Not used

Detailed Description of Supported PMBus Commands

VOUT_MODE (0x20)

Definition: Reports the VOUT mode and provides the exponent used in calculating several VOUT settings.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	1	0	0	1	1
Mode	Bits 7:5	Bits 4:0 (Parameter) `						
Linear	**000**	5-bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.						
Exponent	**10011**	-13 (decimal)						

VOUT_COMMAND (0x21)

Definition: Sets or reports the target output voltage. The range of acceptable values is from 0.45V to V_{OUT_MAX}. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit, a fault will be recorded in STATUS_CML and a warning will be recorded in STATUS_VOUT.

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	VSET/SA Pin-strap Setting															

Units: V

Equation: VOUT = VOUT_COMMAND × 2^{-13}

Range: 0.45V to VOUT_MAX

VOUT_TRIM (0x22)

Definition: Applies a fixed trim voltage to the output voltage command value. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and a fault will be recorded in STATUS_CML.

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Units: V

Equation: VOUT trim = VOUT_TRIM × 2^{-13}

Range: ±0.15V. Default Value 0

VOUT_CAL_OFFSET (0x23)

Definition: Applies a fixed offset voltage to the output voltage command value. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and a fault will be recorded in STATUS_CML. .

Units: V

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Equation: VOUT calibration offset = VOUT_CAL_OFFSET × 2^{-13}

Range: ±0.15V

VOUT_MAX (0x24)

Definition: Sets the upper limit of the output voltage of the module regardless of any other commands or combinations. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and a fault will be recorded in STATUS_CML .

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Equation: VOUT_MAX = VOUT_MAX x 2-13
Range: 0.45V to 5.5V Default value: 2.008V
Units: V

VOUT_MARGIN_HIGH (0x25)

Definition: Sets the value of VOUT during margin high. The command loads the module with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit, a fault will be recorded in STATUS_CML and

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.05 x VSET/SA pin-strap setting															

a warning will be recorded in STATUS_VOUT
Units: V
Equation: VOUT margin high = VOUT_MARGIN_HIGH x 2^{-13}
Range: 0.1V to VOUT_MAX

VOUT_MARGIN_LOW (0x26)

Definition: Sets the value of VOUT during margin low. The command loads the module with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit, a fault will be recorded in STATUS_CML and a warning will be recorded in STATUS_VOUT .

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.95 x VSET/SA pin-strap setting															

Units: V
Equation: VOUT margin low = VOUT_MARGIN_LOWx2^{-13}
Range: 0.1V to VOUT_MAX

VOUT_TRANSITION_RATE(0x27)

Definition: Sets the rate at which the output voltage should change when the module receives an OPERATION command that

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

requires output voltage change. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.
Units: V/ms

Equation: VOUT_TRANSITION_RATE = $Y \times 2^{N}$

Range: 0.1 to 4V/ms. Default Value: 1V/ms

MAX_DUTY (0x32)

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	0

Definition: Sets the maximum allowable duty cycle of the PWM output. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML

Equation: MAX_DUTY = Y x 2N
Range: 0 to 100% Default value: 50%
Units: %

FREQUENCY_SWITCH (0x33)

Definition: Sets the switching frequency of the module. Initial default value is defined by a pin-strap and this value can be over-ridden by writing this command. If an external SYNC is utilized, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command. Available frequencies are defined by the equation fSW = 30MHz/n where 30 ≤ n ≤ 150. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	1	1	0	1	1	1	1	1	0	1	0	0	0

Equation: FREQUENCY_SWITCH = Y x 2N
Range: 200kHz to 1000kHz Default value: 500kHz

POWER_MODE (0x34)

Definition: Enables and disables Diode Emulation Mode (DEM).

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

Bits	Purpose	Bit Value	Meaning
7:1	Not Used	0	Packet Error Checking not supported.
0	Maximum Efficiency	1	Packet Error Checking is supported.

INTERLEAVE (0x37)

Definition: Configures the phase offset of a module that is sharing a common SYNC clock with other modules. Interleaved is used for setting the phase offset between individual modules, current sharing groups, and/or combination of modules and current sharing groups. The offset for modules within single sharing group is set automatically .

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	Last 4 bits of PMBus Address			

Bits	Purpose	Value	Description
15:8	Not Used	0	Not used
7:4	Not Used	0	Not used
3:0	Position in Group (Interleave Order)	0	Sets position of the device's rail within the group. A value of 0 is interpreted as 16. Position 1 has a 22.5 degree offset.

IOUT_CAL_GAIN(0x38)

Definition: Sets the effective impedance across the current sense circuit for use in the calculating output current at +25^{0}C. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	0	1	0	1	0	0	0	0	1	0	1	0	0

Equation: IOUT_CAL_GAIN = Y x 2N
Range: >0mΩ to 1000mΩ Default value: 0.26mΩ

IOUT_CAL_OFFSET(0x39)

Definition: Adjusts the offset in the output current sensing circuit. (Also used to compensate for delayed measurement of current ramp due to the current sensing blanking time. See ISENSE_CONFIG.) If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	0	1	0	1	0	0	0	0	1	0	1	0	0

Equation: IOUT_CAL_OFFSET = Y x 2N
Range: -10A to 10A Default value: 0A
Units: A

VOUT_OV_FAULT_LIMIT(0x40)

Definition: Sets the VOUT overvoltage fault threshold. VOUT_OV_WARN _LIMIT must be set below the VOUT_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When VOUT_OV_FAULT_LIMIT has been exceeded the module will set the VOUT bit in STATUS_WORD, set the VOUT_OV_FAULT bit in STATUS_VOUT, and notifies the host. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit, a fault will be recorded in STATUS_CML and a warning will be recorded in STATUS_VOUT
Units: V

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.1 x VSET/SA pin-strap setting															

Equation: VOUT OV fault limit = VOUT_OV_FAULT_LIMIT × 2^{-13}

Range: 0.45V to 6.0V

VOUT_OV_FAULT_RESPONSE(0x41)

Definition: Configures the V_{OUT} overvoltage fault response. During fault conditions the module may respond to different faults, in which instances the number of retry attempts may appear to be incorrect .

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11 **10**	Not used **Disable Output and retry according to bits [5:3]**
5:3	Retry Setting	001-110	Not used
		111	**Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the output voltage falls below the VOUT_OV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0] multiplied by 35ms.**
		000	No-retry
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VOUT_OV_WARN_LIMIT(0x42)

Definition: Sets the VOUT overvoltage warning threshold. VOUT_OV_WARN_LIMIT must be set below the VOUT_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VOUT_OV_FAULT_RESPONSE is set to retry, a retry will not be attempted until the output voltage has fallen below the VOUT_OV_WARN_LIMIT. When the VOUT_OV_WARN_LIMIT has been exceeded the module sets the VOUT bit in STATUS_WORD, sets the VOUT_OV_WARNING bit in STATUS_VOUT and notifies the host. In the case of a fast VOUT overvoltage transition a VOUT_OV_WARN_LIMIT fault may not be recorded. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and a fault will be recorded in STATUS_CML

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.08x VSET/SA pin-strap setting															

Units: V

Equation: VOUT OV Warn limit = VOUT_OV_WARN_LIMIT × 2^{-13}

Range: 0.45V to 5.5V

VOUT_UV_WARN_LIMIT(0x43)

Definition: Sets the VOUT undervoltage warning threshold. This fault is masked during ramp, before power-good is asserted or when the module is disabled. VOUT_UV_WARN_LIMIT must be set to a value below POWER_GOOD_ON and above VOUT_UV_FAULT_LIMIT. When the VOUT_UV_WARN_LIMIT has been exceeded the module sets the VOUT bit in STATUS_WORD, sets the VOUT_UV_WARNING bit in STATUS_VOUT and notifies the host. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit, a fault will be recorded in STATUS_CML

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.88 x VSET/SA pin-strap setting															

Units: V
Equation: VOUT UV Warn limit = VOUT_UV_WARN_LIMIT × 2^{-13}
Range: 0.45V to 5.5V

VOUT_UV_FAULT_LIMIT(0x44)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp, before power-good is asserted or when the module is disabled. VOUT_UV_FAULT_LIMIT must be set to a value below VOUT_UV_WARN_LIMIT and POWER_GOOD_ON. When the VOUT_UV_FAULT_LIMIT has been exceeded, the module sets the VOUT bit in STATUS_WORD, sets the VOUT_UV_FAULT bit in STATUS_VOUT and notifies the host. If a value

Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.85 x VSET/SA pin-strap setting															

outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and a fault will be recorded in STATUS_CML.

Units: V
Equation: VOUT UV fault limit = VOUT_UV_FAULT_LIMIT × 2^{-13}
Range: 0.45V to 5.5V

VOUT_UV_FAULT_RESPONSE(0x45)

Definition: Configures the VOUT undervoltage fault response. Note that VOUT undervoltage faults can only occur after power-good has been asserted. Under some circumstances this will cause the output to stay fixed below the power-good threshold indefinitely. If this behavior is undesired, use setting 0x80. The retry response will always retry since a faulted state will be, by definition, below the VOUT_UV_WARN threshold. When a fault condition is applied to a rail, due to module timing, it is possible for different faults to trigger the module to shut down. In these cases, the number of retry attempts may appear to be incorrect

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11 **10**	Not used **Disable output and retry according to bits [5:3}**

5:3	Retry Setting	000-110	Not used
		111	**Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the output voltage falls below the VOUT_OV_WARN_LIMIT. The time between the start of each attempt to resta**rt is set by the value in Bits [2:0] multiplied by 35ms.
		000	No-retry
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

IOUT_OC_FAULT_LIMIT(0x46)

Definition: Sets the IOUT peak overcurrent fault threshold. This limit is applied to current measurement samples taken after the current sense blanking time has expired. The fault occurs after this limit is exceeded for the number of consecutive samples as defined in ISENSE_CONFIG. This feature shares the OC fault bit operation in STATUS_IOUT and

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	0	0	1	0	0	0	0	0

MFR_IOUT_OC_FAULT_RESPONSE with IOUT_AVG_OC_FAULT_LIMIT. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.
Units: Amps

Equation: $IOUT\_OC\_FAULT\_LIMIT = Y \times 2^{N}$

Range: 0A to 100A **Default value: 100A**

IOUT_OC_WARN_LIMIT(0x4A)

Definition: Sets the IOUT peak overcurrent warn threshold. This limit is applied to current measurement samples taken after the current sense blanking time has expired. The warn occurs after this limit is exceeded for the number of consecutive samples as defined in ISENSE_CONFIG. When a warn occurs the corresponding bit is set in STATUS_IOUT. If a value outside of the

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0

acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.

Units: Amps

Equation: $IOUT\_OC\_WARN\_LIMIT = Y \times 2^{N}$

Range: 0A to 100A **Default value: 65A**

IOUT_UC_FAULT_LIMIT (0x4B)

Definition: Sets the IOUT valley undercurrent fault threshold. This limit is applied to current measurement samples taken after the current sense blanking time has expired. This feature shares the UC fault bit operation in STATUS_IOUT and IOUT_UC_FAULT_RESPONSE with IOUT_AVG_UC_FAULT_LIMIT. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML .

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	1	0	1	1	1	0	1	0	0	0	0

Units: Amps

Equation: IOUT_UC_FAULT_LIMIT = $Y \times 2^N$ **Default value: -70A**

OT_FAULT_LIMIT (0x4F)

Definition: Sets the temperature at which the module should indicate an over-temperature fault. OT_WARN_LIMIT must be set below the OT_FAULT_LIMIT for fault responses with restart attempts to function properly. When the OT_FAULT_RESPONSE is set to retry, a retry will not be attempted until the temperature has fallen below the OT_WARN_LIMIT. When the OT_FAULT_LIMIT has been exceeded the module sets the TEMPERATURE bit in STATUS_WORD, sets the OT_FAULT bit in STATUS_TEMPERATURE and notifies the host. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML .

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0	0

Units: Degrees Celsius (°C)

Equation: OT_FAULT_LIMIT = $Y \times 2^N$

Range: 0°C to +175°C, Default value: +125°C

OT_FAULT_RESPONSE(0x50)

Definition: Instructs the device on what action to take in response to an over-temperature fault. The delay time is the time between fault detected and restart attempts.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11 **10**	Not used **Disable output and retry according to bits [5:3}**

5:3	Retry Setting	000-110	Not used
		111	**Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the output voltage falls below the VOUT_OV_WARN_LIMIT. The time between the start of each attempt to resta**rt is set by the value in Bits [2:0] multiplied by 35ms.
		000	No-retry
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

OT_WARN_LIMIT (0x51)

Definition: Sets the temperature at which the module should indicate an over-temperature warning alarm. OT_WARN_LIMIT must be set below the OT_FAULT_LIMIT for fault responses with restart attempts to function properly. When the OT_FAULT_RESPONSE is set to retry, a retry will not be attempted until the temperature has fallen below the OT_WARN_LIMIT. When the OT_WARN_LIMIT has been exceeded the module sets the TEMPERATURE bit in STATUS_WORD, sets the OT_WARNING bit in STATUS_TEMPERATURE and notifies the host. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	0	1	1	1	0	0	0	0

Units: Degrees Celsius (°C) Default value: +110°C

Equation: OT_WARN_LIMIT = Y × 2^N Range: 0°C to +175°C

UT_WARN_LIMIT (0x52)

Definition: : Sets the temperature at which the module should indicate an under-temperature fault. UT_WARN_LIMIT must be set above the UT_FAULT_LIMIT for fault responses with restart attempts to function properly. When the UT_FAULT_RESPONSE is set to retry, a retry will not be attempted until the temperature has risen above the UT_WARN_LIMIT. When the UT_FAULT_LIMIT has been exceeded the module sets the TEMPERATURE bit in STATUS_WORD, sets the UT_FAULT bit in STATUS_TEMPERATURE and notifies the host. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	1	0	1	0	0	1	1	0	0	0	0

Units: Degrees Celsius (°C) Default value: -45°C

Equation: UT_WARN_LIMIT = Y × 2^N

Range: -55°C to +25°C

UT_FAULT_LIMIT (0x53)

Definition: : Sets the temperature at which the module should indicate an under-temperature fault. UT_WARN_LIMIT must be set above the UT_FAULT_LIMIT for fault responses with restart attempts to function properly. When the UT_FAULT_RESPONSE is set to retry, a retry will not be attempted until the temperature has risen above the UT_WARN_LIMIT. When the UT_FAULT_LIMIT has been exceeded the module sets the TEMPERATURE bit in STATUS_WORD, sets the UT_FAULT bit in STATUS_TEMPERATURE and notifies the host. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.

Format	11-bit linear

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	1	0	0	1	1	1	0	0	0	0	0

Units: Degrees Celsius (°C)

Equation: UT_FAULT_LIMIT = $Y \times 2^N$

Range: -55°C to + 25°C, Default value: -50^{0}C

UT_FAULT_RESPONSE(0x54)

Definition: Configures the under-temperature fault response.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11 **10**	Not used **Disable output and retry according to bits [5:3}**
5:3	Retry Setting	000-110	Not used
		111	**Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the output voltage falls below the VOUT_OV_WARN_LIMIT. The time between the start of each attempt to resta**rt is set by the value in Bits [2:0] multiplied by 35ms.
		000	No-retry
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

.

VIN_OV_FAULT_LIMIT(0x55)

Definition: Sets the V_{IN} overvoltage fault threshold. VIN_OV_WARN_LIMIT must be set below the VIN_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_OV_FAULT_RESPONSE is set to retry, a retry will not be attempted until the input voltage has fallen below the VIN_OV_WARN_LIMIT. When the VIN_OV_FAULT_LIMIT has been exceeded the module sets the “None of the above” bit in STATUS_BYTE, INPUT and “None of the above” bits in STATUS_WORD, sets the VIN_OV_FAULT bit in STATUS_INPUT and notifies the host. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML

Format	11-bit linear

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0

Units: Volts

Equation: VIN_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0V to 18V, Default value: 16V

VIN_OV_FAULT_RESPONSE(0x56)

Definition: Configures the VIN overvoltage fault response When a fault condition is applied to a rail, due to module timing it is possible for different faults to trigger the module to shut down. In these cases, the number of retry attempts may appear to be incorrect .

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11 **10**	Not used **Disable output and retry according to bits [5:3}**
5:3	Retry Setting	000-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the output voltage falls below the VOUT_OV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0] multiplied by 35ms.
		000	**No-retry**
2:0	Retry Delay	**000**-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VIN_OV_WARN_LIMIT(0x57)

Definition: Sets the V_{IN} overvoltage warning threshold. VIN_OV_WARN_LIMIT must be set below the VIN_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_OV_FAULT_RESPONSE is set to retry, a retry will not be attempted until the input voltage has fallen below the VIN_OV_WARN_LIMIT. When the OV_WARN_LIMIT being exceeded the module sets the NONE_OF_THE_ABOVE and INPUT bits in STATUS_WORD, sets the VIN_OV_WARNING bit in STATUS_INPUT and notifies the host. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML

Format	11-bit linear

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	0	1	1	1	0	1	0	0	0	0	0

Units: Volts

Equation: VIN_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0V to 18V Default value: 14.5V

VIN_UV_WARN_LIMIT(0x58)

Definition: Sets the V_{IN} undervoltage warning threshold. VIN_UV_WARN_LIMIT must be set above the VIN_UV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_UV_FAULT_RESPONSE is set to retry, a retry will not be attempted until the input voltage has risen above the VIN_UV_WARN_LIMIT. When the VIN_UV_WARN_LIMIT being exceeded, the module sets the NONE_OF_THE_ABOVE and INPUT bits in STATUS_WORD, sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.

Format	11-bit linear

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	1	0	1	1	0	0	1	1	0

Units: V

Equation: VIN_UV_WARN_LIMIT = $Y \times 2^N$

Range: 0V to 16V Default value: 6.8V

VIN_UV_FAULT_LIMIT(0x59)

Definition: Sets the V_{IN} undervoltage fault threshold. VIN_UV_WARN_LIMIT must be set above the VIN_UV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_UV_FAULT_RESPONSE is set to retry, a retry will not be attempted until the input voltage has risen above the VIN_UV_WARN_LIMIT. When the VIN_UV_FAULT_LIMIT being exceeded the module sets the NONE_OF_THE_ABOVE and INPUT bits in STATUS_WORD, sets the VIN_UV_FAULT bit in STATUS_INPUT, and notifies the host. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	1	0	1	0	0	0	0	0	0

Units: V

Equation: VIN_UV_FAULT_LIMIT = Y × 2^N

Range: 0V to 16V Default value: 6.5V

VIN_UV_FAULT_RESPONSE (0x5A)

Definition: Configures the V_{IN} undervoltage fault response When a fault condition is applied to a rail, due to module timing it is possible for different faults to trigger the module to shut down. In these cases, the number of retry attempts may appear to be incorrect .

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11 **10**	Not used **Disable output and retry according to bits [5:3]**
5:3	Retry Setting	000-110	Not used
		111	**Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the output voltage falls below the VOUT_OV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0] multiplied by 35ms.**
		000	No-retry
2:0	Retry Delay	**000**-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

POWER_GOOD_ON(0x5E)

Definition: Sets the voltage threshold for power-good indication. Power-Good asserts when the output voltage exceeds POWER_GOOD_ON and de-asserts when the V_{OUT} is less than VOUT_UV_FAULT_LIMIT. POWER_GOOD_ON should be set to a value above VOUT_UV_WARN_LIMIT. Power-Good may not assert if the module is enabled for less than 2ms. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit, a fault will be recorded in STATUS_CML.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.9 x VSET/SA pin-strap setting															

Equation: VOUT_PG_ON = POWER_GOOD_ON x 2-13

Units: Volts Range: 0V to 5.5V

TON_DELAY (0x60)

Definition: Sets the delay time from when the module is enabled to the start of VOUT rise. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML .

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Units: milliseconds (ms)

Equation: TON_DELAY = $Y \times 2^N$

Range: 0ms to 125ms Default value: 0ms

TON_RISE (0x61)

Definition: Sets the rise time of VOUT after the TON_DELAY time has elapsed. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML. Note that although values can be set below 0.50ms, rise time accuracy cannot be guaranteed. In addition, short rise times may cause excessive input and output currents to flow, thus triggering overcurrent faults at start-up.

Units: milliseconds (ms)

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0

Equation: TON_RISE = $Y \times 2^N$

Range: 0ms to 125ms Default value: 4ms

TOFF_DELAY (0x64)

Definition: Sets the delay time from disabling the module to start of VOUT_FALL. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.

Units: milliseconds (ms)

Equation: TOFF_DELAY = $Y \times 2^N$ Default value: 0ms Range: 0ms to 125ms

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TOFF_FALL (0x65)

Definition: Sets the fall time for VOUT after the TOFF_DELAY has expired. Setting the TOFF_FALL to values less than 0.5ms will cause the module to turn-off both the high and low-side FETs immediately after the expiration of the TOFF_DELAY time. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML .

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Units: milliseconds (ms) Default value: 2ms
Equation: TOFF_FALL = $Y \times 2^N$
Range: 0ms to 125ms. .

STATUS_BYTE (0x78)

Definition: Returns a summary of the module's fault condition. Host may get more information from the appropriate status registers.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Description
7	Not Used	Not used
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	Not used	Not used

STATUS_WORD (0x79)

Definition: Returns two bytes of information with a summary of the module's fault condition. Based on the information in these bytes, the host may get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Description
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT	An output current fault has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD #	The POWER_GOOD signal, if present, is negated*
10	NOT USED	Not used
9	OTHER	A bit in STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, or STATUS_MFR_SPECIFIC is set.
8	Not Used	Not used
7	Not Used	Not used
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	Not Used	Not used

* If the POWER_GOOD# bit is set, this indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good. POWER_GOOD may not assert if the device is enabled for less than 2ms.

as the STATUS_BYTE (0x78) command.

STATUS_VOUT (0x7A)

Definition: Returns one data byte with the status of the output voltage. Note that warning bits may not be set when the corre-

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Status Bit Name			Description				
7	VOUT_OV_FAULT			Indicates an output overvoltage fault.				
6	VOUT_OV_WARNING			Indicates an output overvoltage warning. May not be set when an overvoltage fault occurs.				
5	VOUT_UV_WARNING			Indicates an output undervoltage warning. May not be set when an undervoltage fault occurs.				
4	VOUT_UV_FAULT			Indicates an output undervoltage fault.				
3	VOUT_MAX_WARNING			Attempted to set VOUT_COMMAND greater than VOUT_MAX or below 0.1V.				
2:0	Not used			Not used				

sponding fault bits are set. This can occur with rapidly changing fault conditions .

STATUS_IOUT (0x7B)

Definition: Returns one data byte with the status of the output current. Note that warning bits may not be set when the corre-

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Status Bit Name			Description				
7	IOUT_OC_FAULT			An output overcurrent fault has occurred.				
6	Not Used			Not used				
5	IOUT_OC_WARNING			An output overcurrent warning has occurred. May not be set when an output overcurrent fault occurs.				
4	IOUT_UC_FAULT			An output undercurrent fault has occurred.				
3:0	Not Used			Not used				

sponding fault bits are set. This can occur with rapidly changing fault conditions

STATUS_INPUT (0x7C)

Definition: Returns one data byte with the status of the input voltage. Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault conditions

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Status Bit Name			Description				
7	VIN_OV_FAULT			An input overvoltage fault has occurred.				
6	VIN_OV_WARNING			An input overvoltage warning has occurred.				
5	VIN_UV_WARNING			An input undervoltage warning has occurred.				
4	VIN_UV_FAULT			An input undervoltage fault has occurred.				
3:0	Not Used			Not used				

STATUS_TEMPERATURE(0x7D)

Definition: Returns one data byte with the status of the temperature related information. Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault conditions

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Status Bit Name			Description				
7	OT_FAULT			An over-temperature fault has occurred.				
6	OT_WARNING			An over-temperature warning has occurred.				
5	UT_WARNING			An under-temperature warning has occurred.				
4	UT_FAULT			An under-temperature fault has occurred.				
3:0	Not Used			Not used				

STATUS_CML (0x7E)

Definition: Returns one byte of information with a summary of any communications, logic, and/or memory errors. Status bits can only be cleared with the CLEAR_FAULTS command or by disabling, then re-enabling the device.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Description							
7	Invalid or unsupported PMBus command was received.							
6	The PMBus command was sent with invalid or unsupported data.							
5	A Packet Error Check (PEC) failed on a PMBus command.							
4:2	Not used							
1	A PMBus command tried to write to a read only or protected command, or too few or too many bytes were received for a given command.							
0	Not used							

STATUS_MFR_SPECIFIC(0x80)

Definition: Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bit Number	Status Bit Name			Description				
7	Not Used			Not used				
6	Phase Fault			A phase in the current sharing group has failed, when configured as part of a current sharing rail.				
5	Not Used			Not used				
4	DDC fault			An error was detected on the DDC bus.				
3	External Switching Period Fault			Loss of external clock synchronization has occurred.				
2	Fault Group			A fault was spread using DDC fault group				
1	Not Used			Not used				
0	Fault Bus			Module was shut down by the ON/OFF pin when using the ON/OFF pin as a fault bus				

Detailed Description of Supported PMBus Commands

READ_VIN (0x88)

Definition: Returns the input voltage reading.

Format	11-bit linear

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X

Units: V

Equation: READ_VIN = $Y \times 2^{N}$

READ_IIN (0x89)

Definition: Returns the input current reading. The reading is not accurate when the module is in Diode Emulation Mode (DEM). It is calculated using the values of the output current, duty cycle, and IIN_CAL_OFFSET.

Format	11-bit linear

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X

Units: A

Equation: READ_IIN = $Y \times 2^{N}$

READ_VOUT (0x8B)

Definition: Returns the output voltage reading.

Format	11-bit linear

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X

Units: V

Equation: READ_VOUT = READ_VOUT $\times 2^{-13}$

READ_IOUT (0x8C)

Definition: Returns the output current reading. The reading is not accurate when the module is in Diode Emulation Mode (DEM). No reading is returned when the output is not being regulated .

Units: A

Equation: READ_IOUT = $Y \times 2^{N}$

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X

READ_TEMPERATURE_1(0x8D)

Definition: Returns the temperature of the controller die .

Units: °C

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X

Equation: READ_TEMPERATURE_1 = Y × 2^N

READ_DUTY_CYCLE(0x94)

Definition: Reports the actual duty cycle of the converter while the device is enabled.

Units: %

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X

Equation: READ_DUTY_CYCLE = Y × 2^N

READ_FREQUENCY (0x95)

Definition: Reports the actual configured switching frequency of the device.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X

Units: kHz

Equation: READ_FREQUENCY = Y × 2^N

Detailed Description of Supported PMBus Commands

READ_POUT (0x96)

Definition: Returns the calculated output power in Watts.

Format	11-bit linear

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X

Units: W

Equation: READ_POUT = $Y \times 2^N$

READ_PIN (0x97)

Definition: Returns the calculated input power in Watts.

Format	11-bit linear

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	X

Units: W

Equation: READ_PIN = $Y \times 2^N$

PMBUS_REVISION (0x98)

Definition: Returns the revision of the PMBus Specification to which the device is compliant

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	1	1	0	0	1	1

Bits 7:4	Bits 3:0
0011	0011
Part 1 Revision 1.3	Part 2 Revision 1.3

Default Value: 33h (Part 1 Revision 1.3, Part 2 Revision 1.3)

IC_DEVICE_ID (0xAD)

Definition: Reports controller identification information (4 bytes block read)

Format	Block Read			
Byte Position	3	2	1	0
Access	R	R	R	R
Function	Reserved	ID Low Byte	ID High Byte	MFR Code
Default Value	0x00	0x31	0xA0	0x49

IC_DEVICE_REV (0xAE)

Definition: Reports controller revision information (4 bytes block read)

Format	Block Read			
Byte Position	3	2	1	0
Access	R	R	R	R
Function	FW Minor	FW Major	Interface Minor	Interface Major
Default Value	0x05	0x09	0x00	0x09

USER_DATA_00 (0xB0)

Definition: Sets a user defined data string not to exceed 17 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Format: ASCII. ISO/IEC 8859-1

USER_DATA_01 (0xB1)

Definition: Sets a user defined data string not to exceed 17 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Format: ASCII. ISO/IEC 8859-1

USER_DATA_02 (0xB2)

Definition: Sets a user defined data string not to exceed 17 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Format: ASCII. ISO/IEC 8859-1

ISENSE_CONFIG (0xD0)

Definition: Configures current sense circuitry . This command is Read Only

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						See below										
Default Value	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0

Bits 15:11 Current sense circuit blanking time in increments of 32ns.
- 00000 0ns blanking time
- 11010 832ns. Longer blanking time is not supported

Bits 10:8 Current sense fault count. Number of consecutive OC or UC events required for a fault to be declared. An event can occur once during a switching cycle. Equation: Count = 2 x Value + 1
- 000 1 consecutive cycle under fault condition
- 001 3 consecutive cycles under fault condition
- 111 15 consecutive cycles under fault condition

Bits 7:3 Not used

Bit 2 Sets the slope at which the current will be sampled.
- 0 Down slope
- 1 Up slope

Bits 1:0 Current sense range
- 00 Low range ±15mV
- 01 Medium range ±30mV
- 10 High range ±60mV
- 11 Not used

USER_CONFIG (0xD1)

Definition: Configures several user-level features. This command should be saved immediately after being written to the desired user or default store. This is recommended when written as an individual command or as part of a series of commands in a configuration file or script.

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0

Bits	Field Name	Value	Setting	Description
15:11	Minimum Duty Cycle	00000	0-31d	Set the Minimum Duty Cycle in percent (%). The percentage value is defined by the following expression: Minimum Duty Cycle = 2 X (Setting+1) / 512. This feature must be enabled by setting Bit 10 to 1 (enabled).
10	Minimum Duty Cycle Enable	0	Disable	Minimum duty cycle disabled
		1	Enable	Minimum duty cycle enabled
9	DEM Boot Cap Refresh	0	Disable	Low-side gate minimum pulse width disabled
		1	Enable	Low-side gate minimum pulse width enabled during diode emulation mode. This ensures that the top FET bootstrap capacitor is recharged every switch cycle.
8	Not Used	0	Not Used	Not used
7	Enable Fault Bus	0	Disable	Disable Fault Bus
		1	Enable	Enable Fault Bus
6	Not Used	0	Not Used	Not used
5	Power-Good Pin Configuration	0	Open Drain	0 = PG is open-drain output
		1	Push-Pull	1 = PG is push-pull output
4:3	Temp Fault Select	00	Internal temperature sensor selected	Select internal temperature sensor to determine temperature faults.
		01-11	Not Used	Not used
2	Not Used	0	Not Used	Not used
1:0	Sync Pin Configuration	00	Internal Clock	Use internal clock (frequency initially set with pin-strap)
		01	Use and Output Internal Clock	Use internal clock and output internal clock (not for use with pin-strap)
		10	External Clock	Use external clock
		11	Not Used	Not used

DDC_CONFIG (0xD3)

Definition: Configures DDC addressing and current sharing for up to eight phases. To operate as a 2-phase controller, set both phases (devices) to the same rail ID, set phases in rail to 2, then set each phase ID sequentially as 0 and 1. The devices automatically equally offset the phases in the rail. For example, in a 2-phase rail the phases are offset by 180 degrees. When a device is configured to be part of a current sharing rail, DDC_GROUP must be configured such that all phases in the current sharing rail have the same DDC_GROUP ID and are set to respond to DDC_GROUP OPERATION and VOUT COMMAND messages. See the DDC_GROUP command for more details.

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	Lower 5 bits of device address					0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
15:13	Phase ID	0 to 7	0	Sets the output's phase position within the rail
12:8	Rail ID	0 to 31d	0	Identifies the device as part of a current sharing rail (Shared output)
7:3	Not Used	00	00	Not used
2:0	Phases In Rail	0 to 7	0	Identifies the number of phases on the same rail (+1)

POWER_GOOD_DELAY(0xD4)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 125ms. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

Units: milliseconds (ms)

Equation: POWER_GOOD_DELAY = $Y \times 2^N$

Range: 0ms to 125ms. Default value 1ms

ASCR_ADVANCED (0xD5)

Definition: Allows user configuration of advanced ASCR settings which have an impact on PWM jitter. ASCR threshold setting sets the level at which the output voltage is deemed to be at steady state. ASCR threshold gain reduction sets the amount by which the ASCR gain is reduced when the output voltage is deemed to be in the steady state

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used		ASCR TH Gain Setting			ASCR Threshold Setting										
Default Value	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Purpose	Value	Description
15:14	Not used	00	Not used
13:12	ASCR Threshold Gain Select Setting	00	Divide by 1
		01	Divide by 2
		10	Divide by 4
		11	Divide by 8
11:0	ASCR Threshold Setting		ASCR Threshold

INDUCTOR (0xD6)

Definition: This is a READ only command. It Informs the controller of the converter's inductor value. This is used in adaptive algorithm calculations relating to the inductor ripple current. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	0	0	0	1	0	1	1	1	1	0	1	0	1

Equation: $L = Y \times 2^{N}$

Default value 0.185µH

Detailed Description of Supported PMBus Commands

SNAPSHOT_FAULT_MASK(0xD7)

Definition: Prevents faults from causing a SNAPSHOT event (and store) from occurring. This is a Read Only Command

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Description
15	Fault Phase	Ignore phase faults in a current sharing rail
14	Fault Group	Ignore rail faults in a fault spreading group
13	Fault CPU	Ignore CPU faults
12	Fault UT	Ignore under-temperature faults
11	Fault OT	Ignore over-temperature faults
10	Fault peak OC	Ignore peak output overcurrent faults
9	Fault peak UC	Ignore peak output undercurrent faults
8	Fault EN pin as fault bus	Ignore Enable pin faults when the Enable pin is used as a fault bus
7	Fault VIN_OV	Ignore input overvoltage faults
6	Fault VOUT_OV	Ignore output overvoltage faults
5	Fault VOUT_UV	Ignore output undervoltage faults
4	Not Used	Not Used
3	Fault Sync	Ignore loss of synchronization faults
2	Fault VIN_UV	Ignore Input undervoltage faults
1	Fault IOUT_OC	Ignore output average overcurrent faults
0	Fault IOUT_UC	Ignore output average undercurrent faults

OVUV_CONFIG (0xD8)

Definition: Configures the output voltage OV and UV fault detection parameters.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	1	0

Bits	Purpose	Bit Value	Description
7:4	Not Used	0	Not used
3:0	Defines the number of consecutive limit violations required to declare an OV or UV fault	N	N+1 consecutive OV or UV violations initiate a fault response

MFR_SMBALERT_MASK(0xDB)

Definition: Used to prevent faults from activating the SALRT pin. The bits in each byte correspond to a specific fault type as defined in the STATUS command.. This is a READ Only Command

Format	Bit Field							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Bit Position	55	54	53	52	51	50	49	48
Default Value Byte 6	0	0	0	0	0	0	0	0
Bit Position	47	46	45	44	43	42	41	40
Default Value Byte 5	0	0	0	0	0	0	0	0
Bit Position	39	38	37	36	35	34	33	32
Default Value Byte 4	0	0	0	0	0	0	0	0
Bit Position	31	30	29	28	27	26	25	24
Default Value Byte 3	0	0	0	0	0	0	0	0
Default Value Byte 3	0	0	0	0	0	0	0	0
Bit Position	23	22	21	20	19	18	17	16
Default Value Byte 2	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8
Default Value Byte 1	0	0	0	0	0	0	0	0
Bit Position	7	6	5	4	3	2	1	0
Default Value Byte 0	0	0	0	0	0	0	0	0

Byte	Status Byte Name	Description
6	STATUS_MFR_SPECIFIC	Mask manufacturer specific faults as identified in the STATUS_MFR_SPECIFIC byte.
5	STATUS_OTHER	Not used
4	STATUS_CML	Mask communications, memory or logic specific faults as identified in the STATUS_CML byte.

3	STATUS_TEMPERATURE	Mask temperature specific faults as identified in the STATUS_TEMPERATURE byte
2	STATUS_INPUT	Mask input specific faults as identified in the STATUS_INPUT byte
1	STATUS_IOUT	Mask output current specific faults as identified in the STATUS_IOUT byte
0	STATUS_VOUT	Mask output voltage specific faults as identified in the STATUS_VOUT byte

TEMPCO_CONFIG (0xDC)

Definition: Configures the correction factor and temperature measurement source when performing temperature coefficient correction for current sense. TEMPCO_CONFIG values range from 0 to 127, representing 100 parts per million (ppm) temperature coefficient of resistance. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML

Format	**Bit Field**							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Below							
Default Value	0	0	1	0	1	1	0	0

Bit 7 Selects the temperature sensor source for temperature compensation
- 0 Internal temperature sensor
- 1 Illegal. No external temperature sensor

Bits 6:0 Sets the temperature correction for IOUT_CAL_GAIN in increments of 100ppm/°C

Equation: $IOUT\_CAL\_GAIN_{COMPENSATED} = IOUT\_CAL\_GAIN_{@25°C} * [1 + TEMPCO\_CONFIG(6:0) * 10^{-6} * (Measured\ Temperature - 25°C)]$

Range: 0 to 12700 ppm/°C

Default value: 4400 ppm/°C

DEADTIME(0xDD)

Definition: Sets the non-overlap between PWM transitions using a 2-byte data field. The most significant byte controls the high-side to low-side deadtime time value. The least-significant byte controls the low-side to high-side deadtime value. Negative values are not allowed

Format	**Two 8-bit 2's compliment fields**															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/w	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	High-side to low-side deadtime								Low-side to high-side deadtime							
Default Value	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0

Equation: TIME = Y
Range: 0ns to 60ns.
Default value 20ns/20ns

ASCR_CONFIG (0xDF)

Definition: Allows user configuration of ASCR settings. ASCR gain and residual value are automatically set by the controller based on input and output voltages. ASCR Gain is analogous to bandwidth, ASCR Residual is analogous to damping factor. To improve load transient response performance, increase ASCR Gain. Increasing ASCR Residual to lower transient response overshoot and improve transient response damping. Changing ASCR Residual will not affect the peak output voltage deviation but it will result in slower recovery times. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Typical ASCR Gain settings range from 100 to 1000, and typical ASCR Residual settings range from 10 to 90 .

Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Integral Gain								ASCR Residual							
Default Value	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	ASCR Gain															
Default Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Purpose	Value	Description
31:24	Integral Gain	0-7Fh	Error signal gain
23:16	ASCR residual	0-7Fh	ASCR residual
15:0	ASCR gain	0-FFFFh	ASCR gain

Default value: 0x804000FF (Integral Gain = 128, Residual = 64, ASCR gain = 255)

SEQUENCE (0xE0)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multi-rail sequencing. The module will enable its output when its ON/OFF pin or OPERATION enable state, as defined by ON_OFF_CONFIG, is set and the prequel module has issued a power-good event on the DDC bus as a result of the prequel's Power-Good (PG) signal going high. The module will disable its output (using the programmed delay values) when the sequel module has issued a power-down event on the DDC bus at the completion of its ramp-down (its output voltage is 0V). Fault spreading is not automatic in modules that have a prequel or sequel. When a module shuts down due to a fault, it will not disable its output and will not send a message to its sequel or prequel to disable. If fault spreading behavior is desired, the DDC_GROUP or LEGACY_FAULT_GROUP commands should be used. Automatic fault retry is not supported for fault spreading or sequencing groups

Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
15	Prequel Enable	0	Disable	Disable,
		1	Enable	Enable, prequel to this rail is defined by Bits 12:8
14:13	Not Used	0	Not Used	Not used
12:8	Prequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the prequel rail
7	Sequel Enable	0	Disable	Disable,
		1	Enable	Enable, sequel to this rail is defined by Bits 4:0
6:5	Not Used	0	Not Used	Not used
4:0	Sequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the sequel rail

TRACK_CONFIG (0xE1)

Definition: Configures the voltage tracking modes of the module. When tracking, the TOFF_DELAY in the tracking module must be greater than TOFF_DELAY + TOFF_FALL in the module being tracked. When configured to track, VOUT_COMMAND must be set to the desired steady state output voltage. Module that is providing the tracking signal and the module that tracks it must have their ON/OFF pins tied together. If the OPERATION command is used to enable modules, then DDC_GROUP must be configured on both modules with the same BROADCAST_OPERATION group ID (Bits 12:8) and have BROADCAST_OPERATION response enabled (Bit 13 set to 1)).

Pre-biasedtracking: The circuit tracking the voltage applied to the SEQ pin will slew to whatever voltage is present at the pin when the tracking function is enabled. Depending on how much pre-bias voltage is present on the SEQ pin, the output voltage may overshoot, or an overcurrent fault may occur as the module attempts to rapidly track to this voltage. For this reason, it is recommended that pre-bias voltage on the SEQ pin be no more than 20% of the desired steady state output voltage.

Sequencing: A tracking module cannot be part of a sequencing group; it cannot be a prequel or sequel .

Margining: VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW do not apply to modules that are configured for tracking .

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0
Bits	Field Name		Value	Setting	Description			
7	Voltage Tracking Control		0	Disable	**Tracking is disabled.**			
			1	Enable	Tracking is enabled.			
6	Internal Low Pass Filter		0	Disable	**Filter is disabled**			
			1	Enable	Filter is enabled			
5:3	Not Used		000	Not Used	Not used			
2	Tracking Ratio Control		**0**	**100%**	**Output tracks at 100% ratio of VTRK input.**			
			1	50%	Output tracks at 50% ratio of VTRK input.			
1	Target Limit		**0**	**Target Voltage**	**Output voltage is limited by target voltage.**			
			1	VTRK Voltage	Output voltage is limited by VTRK voltage.			
0	Not Used		0	Not Used	Not used			

DDC_GROUP (0xE2)

Definition: Rails (output voltages) are assigned Group numbers to share specified behaviors. The DDC_GROUP command configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT_COMMAND group ID and enable. Note that DDC Groups are separate and unique from DDC Rail IDs (see DDC_CONFIG). Current sharing rails must be in the same DDC Group to respond to broadcast VOUT_COMMAND and OPERATION commands. Modules in a current sharing rail are not required to have the same POWER_FAIL group ID. Faults are automatically spread when a module is configured to be part of a current sharing rail. If it is desirable the current sharing rail to spread faults with another rail, then all the modules in that current sharing rail should have the same POWER_FAIL group ID as the rail it is expected to share POWER_FAIL faults with. Automatic fault retry behavior is not supported for fault spreading or sequencing groups. When a module is set to ignore DDC GROUP messages, the module will still transmit DDC messages with its own DDC ID. Note that the default DDC_GROUP ID is set to 0d, which is a valid DDC_GROUP number, so even a module with the default setting (ignore all DDC groups, all DDC group IDs set to 0d) will still transmit DDC GROUP messages, despite ignoring DDC_GROUP messages from other modules on the DDC bus .

Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used										EN	VOUT_COMMAND Group ID				
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used		EN	OPERATION Group ID					Not Used		EN	Power Fail Group ID				
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Purpose	Value	Description
31:22	Not Used	00	Not used
21	BROADCAST_VOUT_COMMAND response	1	Responds to broadcast VOUT_COMMAND with same Group ID
		0	Ignores broadcast VOUT_COMMAND
20:16	BROADCAST_VOUT_COMMAND group ID		
15:14	Not Used	00	Not used
13	BROADCAST_OPERATION response	1	Responds to broadcast OPERATION with same Group ID
		0	Ignores broadcast OPERATION
12:8	BROADCAST_OPERATION group ID		
7:6	Not Used	00	Not used
5	POWER_FAIL response	1	Responds to POWER_FAIL events with same Group ID
		0	Ignores POWER_FAIL events with same Group ID
4:0	POWER_FAIL group ID		Group ID sent as data for broadcast POWER_FAIL events

Default value: 0x00000000 (DDC groups not used)

STORE_CONTROL(0xE3)

Definition: Used to store command settings in the USER and DEFAULT stores while the module is enabled. Used in conjunction with STORE_DATA.

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Below							
Default Value	0	0	0	1	0	0	0	0

Bits 7:4 Store to be read from or written to
0001 User store
0010 Default store
0000, 0011 – 1111 Not used

Bits 3:0 Command
0000 Read store

0001 Erase Store
0010 Start write
0011 End write
0100 – 1111 Not used

DEVICE_ID(0xE4)

Definition: Returns the 16-byte (character) module identifier string. The format is: Part Number, Release Type Letter, Major Revision, Minor Revision. .

Format	16-byte string															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Below															
Default Value	5	0	9	0	E	-	0	-	4	1	3	8	6	L	S	I

Bytes 15:14 Minor revision

Bytes 13:12 Major revision

Byte 11 Rel. Type?

Byte 10 ?

Bytes 9:0 Part number

MFR_IOUT_OC_FAULT_RESPONSE(0xE5)

Definition: Configures the IOUT overcurrent fault response as defined by the table below. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT .

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	0	0

Bits	Purpose	Bit Value	Description
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Not used.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used

		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

MFR_IOUT_UC_FAULT_RESPONSE(0xE6)

Definition: Configures the IOUT undercurrent fault response as defined by the table below. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT .

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	0	1	0
Bits	Purpose			Bit Value	Description			
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.			00	Not used			
				01	Not used			
				10	Disable without delay and retry according to the setting in Bits 5:3.			
				11	Not used.			
5:3	Retry Setting			000	No retry. The output remains disabled until the fault is cleared.			
				001-110	Not used			
				111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits [2:0].			
2:0	Retry Delay			000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.			

IOUT_AVG_OC_FAULT_LIMIT(0xE7)

Definition: Sets the IOUT average overcurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the D interval). This feature shares

the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_ OC_FAULT_LIMIT. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML.

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	0	0	1	0	1	1	0	0	0

Units: A

Equation: IOUT_AVG_OC_FAULT_LIMIT $= Y \times 2^N$

Range: 0A to 100A, Default Value=75A

IOUT_AVG_UC_FAULT_LIMIT(0xE8)

Definition: Sets the IOUT average undercurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the D interval). This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_ UC_FAULT_LIMIT If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML .

Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	1	0	0	1	1	1	0	0	0	0	0

Units: A

Equation: IOUT_AVG_UC_FAULT_LIMIT $= Y \times 2^N$

Range: -100A to 0 A Default Value=-50A

SNAPSHOT (0xEA)

Definition: This is a READ only Command. It is a 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash either during a fault condition or through a system-defined time using the SNAPSHOT_CONTROL command. Snapshot is continuously updated in RAM and can be read using the SNAPSHOT command. When a fault occurs, the latest snapshot in RAM is stored to flash. Snapshot data can be read back by writing a 0x01 to the SNAPSHOT_CONTROL command, then reading SNAPSHOT.

Byte	Value	PMBus Command	Format
31:30	Duty Cycle	READ_DUTY_CYCLE (94h)	2 Byte Linear-11
29:28	Switching Frequency	READ_FREQUENCY (95h)	2 Byte Linear-11
27:26	External Temperature 2 (TMON)	READ_TEMPERATURE_3 (8Fh)	2 Byte Linear-11
25:24	External Temperature 1	READ_TEMPERATURE_2 (8Eh)	2 Byte Linear-11
23:22	Internal Temperature	READ_TEMPERATURE_1 (8Dh)	2 Byte Linear-11
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	1 Byte Bit Field
20	CML Status Byte	STATUS_CML (7Eh)	1 Byte Bit Field
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	1 Byte Bit Field
18	Input Status Byte	STATUS_INPUT (7Ch)	1 Byte Bit Field
17	IOUT Status Byte	STATUS_IOUT (7Bh)	1 Byte Bit Field
16	VOUT Status Byte	STATUS_VOUT (7Ah)	1 Byte Bit Field
15:14	Highest Measured Output Current	N/A (Peak measured output current)	2 Byte Linear-11
13:12	Output Current	READ_IOUT (8Ch)	2 Byte Linear-11
11:10	Output Voltage	READ_VOUT (8Bh)	2 Byte Linear-16 Unsigned
9:8	Input Voltage	READ_VIN (88h)	2 Byte Linear-11
7:6	All Faults	N/A	2 Byte Bit Field
5	First Fault	N/A	1 Byte Bit Field
4:1	Uptime	N/A	4 Byte Integer
0	Flash Memory Status Byte	N/A	1 Byte Bit Field

BLANK_PARAMS (0xEB)

Definition: Returns a 32-byte string that indicates which parameter values were retrieved by the last RESTORE operation or have been written since that time. Read BLANK_PARAMS immediately after a restore operation to determine which parameters are in that store. A bit set to “1” indicates the parameter is not present and has not been written since the RESTORE operation. The 32-byte string, 256 bits, corresponds to the 256 possible PMBus commands: from 0x00 to 0xFF. Each bit references a PMBus command by command number, for example ON_OFF_CONFIG, command 0x02 corresponds to bit 2. If the setting of ON_OFF_CONFIG was changed and stored in the USER or DEFAULT stores, the last 2 bytes of BLANK_PARAMS would be 1111 1011

STORE_DATA (0xF2)

Definition: Stores the command settings in the USER and/or DEFAULT stores while the module is enabled. Used in conjunction with STORE_CONTROL (0xE3). This command indicates to the module that the next 4 bytes are PMBus command codes and/or data. STORE_DATA commands, along with their 4 bytes of data, are repeatedly sent to the module until all configuration commands and data have been sent to the module. If the data that needs to be sent results in a STORE_DATA command that would have less than 4 bytes, the unused bytes should be filled with 0xFF. Note that these “filler” bytes will be used when the CRC is calculated

SNAPSHOT_CONTROL (0xF3)

Definition: Controls, configures, and erases SNAPSHOT data. As shown in the table below, this command is used to arm and disarm SNAPSHOT, report back the number of SNAPSHOT data record locations that are available for new data, select the data record to read back, specify whether a single or multiple SNAPSHOT should be taken after a module has been disabled, if a SNAPSHOT can only

be taken when the module is enabled, enabling and disabling SNAPSHOT_CONTROL, and erasing all SNAPSHOT data. The Erase All bit must be sent as a separate command. All other bits will be ignored when the Erase All bit is sent. For example, 0000 0000 0000 0010b and 1111 1111 1111 1111b will both (only) erase all SNAPSHOT data. The host must wait at least 20ms before issuing any other PMBus commands after writing the Erase All bit .

The Erase All bit must be sent as a separate command. All other bits are ignored when the Erase All bit is sent. For example, 0000 0000 0000 0010b and 1111 1111 1111 1111b both (only) erase all SNAPSHOT data. The hose must wait at least 20ms before issuing any other PMBus commands after writing the Erase All bit.

Format	Bit/Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
15	Snapshot Armed	0	Disabled	Not Armed
		1	Enabled	Armed. Snapshot happens on next fault (provided it is not masked)
14:12	Not Used	000	Not Used	Not used
11:8	Available Snapshots	0000-1000	N/A	Number of 8 byte SNAPSHOT records available
7	One Time	0	Disabled	Snapshot is taken whenever a fault occurs
		1	Enabled	One Snapshot is taken when a fault occurs. Another Snapshot is not taken until the device has been disabled.
6	After Enable	0	Disabled	Snapshot may be taken at any time.
		1	Enabled	Snapshot is only taken when the device is enabled (“turned on”)
5	Not used	0	Not used	Not used
4:2	Read Location	000-111	NA/	Specifies which SNAPSHOT data record to return when the SNAPSHOT command is read.
1	Erase All	1	(Write Only)	Erases all SNAPSHOT data. This causes Available Snapshots Remaining to become 8 (1000d) THIS BIT MUST BE SENT AS A SEPARATE COMMAND; such as, not combined with other bit settings.
0	Enable	0	Disabled	Disables SNAPSHOT_CONTROL
		1	Enabled	Enables SNAPSHOT_CONTROL

PINSTRAP_READ_STATUS (0xF5)

Definition: A 5-byte read-back of an index from 0 to 31 that corresponds to the resistor value for the designated pin-strap position.

Byte	Value	Format
Byte 4	Reserved	8-Bit Integer
Byte 3	Reserved	8-Bit Integer
Byte 2	SYNC resistor index	8-Bit Integer
Byte 1	Factory Mode	8-Bit Integer
Byte 0 Bits 7:3	VSET/SA VSET resistor index	5-Bit Integer
Byte 0 Bits 2:0	VSET/SA Address resistor index	3-Bit Integer

IIN_CAL_OFFSET (0xF6)

Definition: Used to account for input current that is consumed by the control circuit. If a value outside of the acceptable range is written to this command, the module will set the value equal to the lower or the upper limit and fault will be recorded in STATUS_CML

Equation: IIN_CAL_OFFSET = $Y \times 2^N$

Range: 10A to 10A, Default Value=0A

SECURITY_CONTROL(0xFA)

Definition: Reads back the security status of the USER and DEFAULT stores, clears protection status of non-password protected commands, and enables the automatic command protection mode (Auto Protect Mode). SECURITY_CONTROL is used along with the PASSWORD and WRITE_PROTECT commands to allow the user to disallow changes to selected commands

Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bits	Field Name	Bit Value	Description
7:6	Not used	00	Not used
5	DEFAULT store protected	0	1 indicates that the DEFAULT store is protected.
4	USER store protected	0	1 indicates that the USER store is protected.
3:2	Not used	00	Not used.
1	Clear protected	0	Writing a “1” clears all protected commands except the commands that are password protected.
0	Auto protect	0	Writing a “1” enables auto protection mode.

PASSWORD (0xFB)

Definition: Sets Sets the password string for the USER and DEFAULT stores. The USER and DEFAULT stores can have unique passwords. The initial (default) passwords for both stores are null (9 bytes of zeroes in hexadecimal format - not 9 ASCII “0” characters). The DEFAULT store password has priority over the USER store password. That is, when the DEFAULT store password is written, protected commands in both the DEFAULT and USER stores can be written to.
Data Format: ASCII. ISO/IEC 8859-1

WRITE_PROTECT (0xFD)

Definition: Sets a 256-bit (32-byte) parameter which identifies which commands are to be protected against write-access. Each bit in this parameter corresponds to a command according to the command's code. The command with a code of 00h (PAGE - not used in this module) is protected by the least-significant bit of the least-significant byte, followed by the command with a code of 01h and so forth. Note that all possible commands have a corresponding bit regardless of whether they can be protected or are supported by the module. Setting a command's WRITE_PROTECT bit to "1" indicates that write-access to that command is only allowed if the appropriate password has been written to the module. Note that the USER and DEFAULT stores have unique passwords, and that writing the DEFAULT store password will allow changes to both the USER and DEFAULT stores.

This page is left intentionally blank to mark the end of a section.

Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation. Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Figure 35a. The preferred airflow direction for cooling the module and the thermal reference points, Tref used in the specifications are shown in Figure 35b. For reliable operation the temperatures at these points should not exceed 115°C (C17 and C6). The output power of the module should not exceed the rated power of the module (Vo,set x Io,max). Please refer to the Application Note “Thermal Characterization Process for Open-Frame Board-Mounted Power Modules” for a detailed discussion of thermal aspects including maximum device temperatures. Increased airflow over the module enhances the heat transfer via convection. The thermal derating of figures 2, 8, 14, 20 and 26 show the maximum output current that can be delivered by each module in the indicated orientation without exceeding the maximum Tref temperature versus local ambient temperature (T_A) for several air flow conditions.

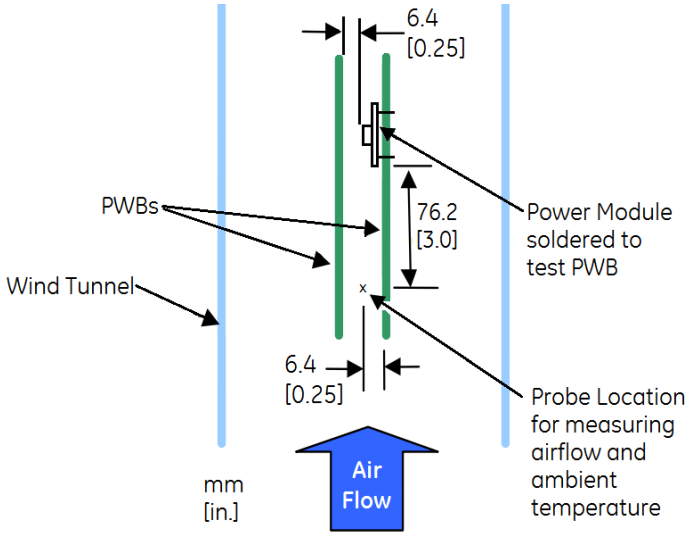

Figure 35a. Thermal testing setup

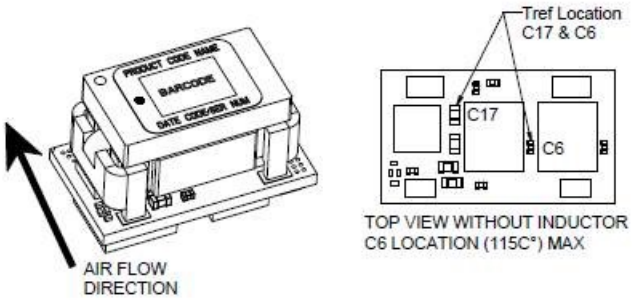

Figure 35b. Preferred airflow direction and the location of the thermal reference points

Example Application Circuit

Requirements:

Vin: 12V

Vout: 1.2V

Iout: 60A max.

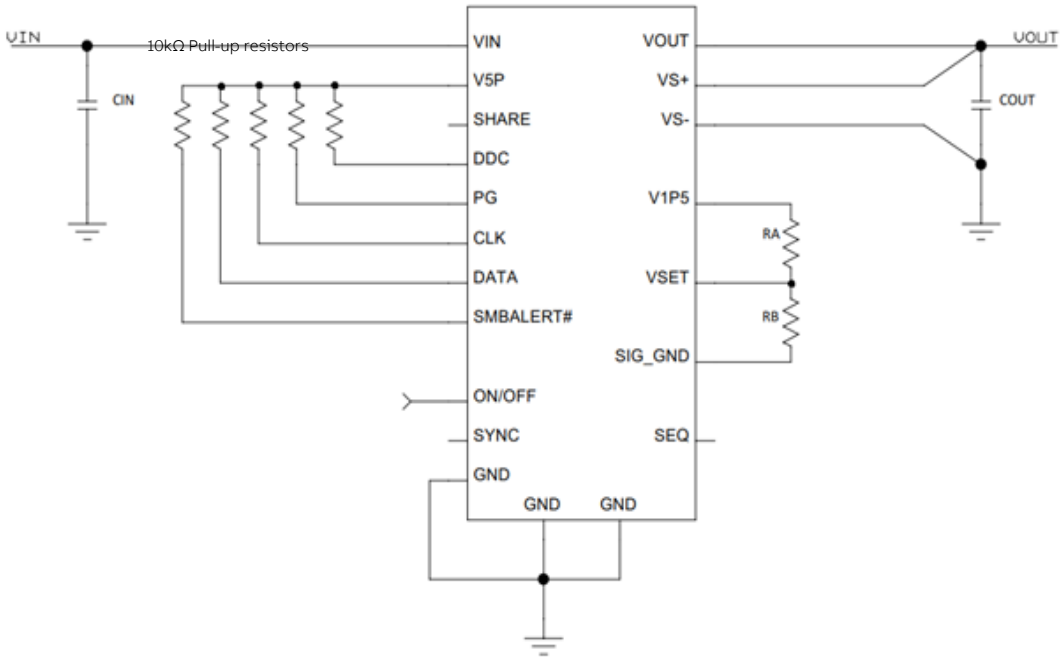

Figure 36. Example Application Circuit

Cin	3 x 0.1uF(ceramic) || 4 x 10uF (ceramic) || 10 x 22uF (ceramic) || 2 x 470uF (Aluminum Polymer)
Cout	4 x 0.1uF (ceramic) || 12 x 47uF (ceramic) || 4 x 680uF (Tantalum Polymer)
RA	392kΩ
RB	38.3kΩ

ASCR Controller Settings:

ASCR Gain = 255

ASCR Integral = 128

ASCR Residual = 64

Steady State Gain Reduction = 4

Threshold = 255

Mechanical Outline

Dimensions are in millimeters and (inches).

Tolerances: x.x mm ± 0.5 mm (x.xx in. ± 0.02 in.) [unless otherwise indicated]

x.xx mm ± 0.25 mm (x.xxx in ± 0.010 in.)

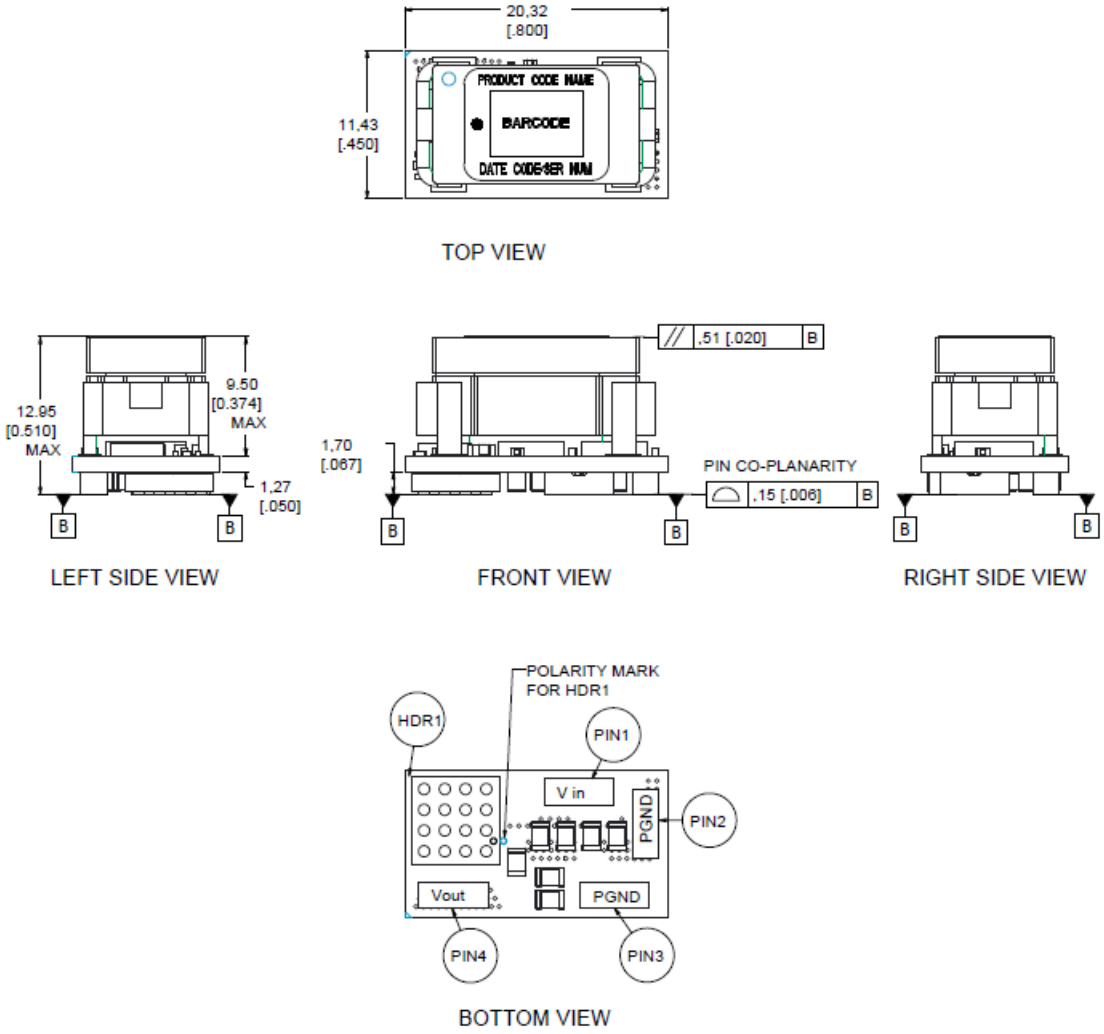

Figure 37. Physical dimensions

Recommended Pad Layout

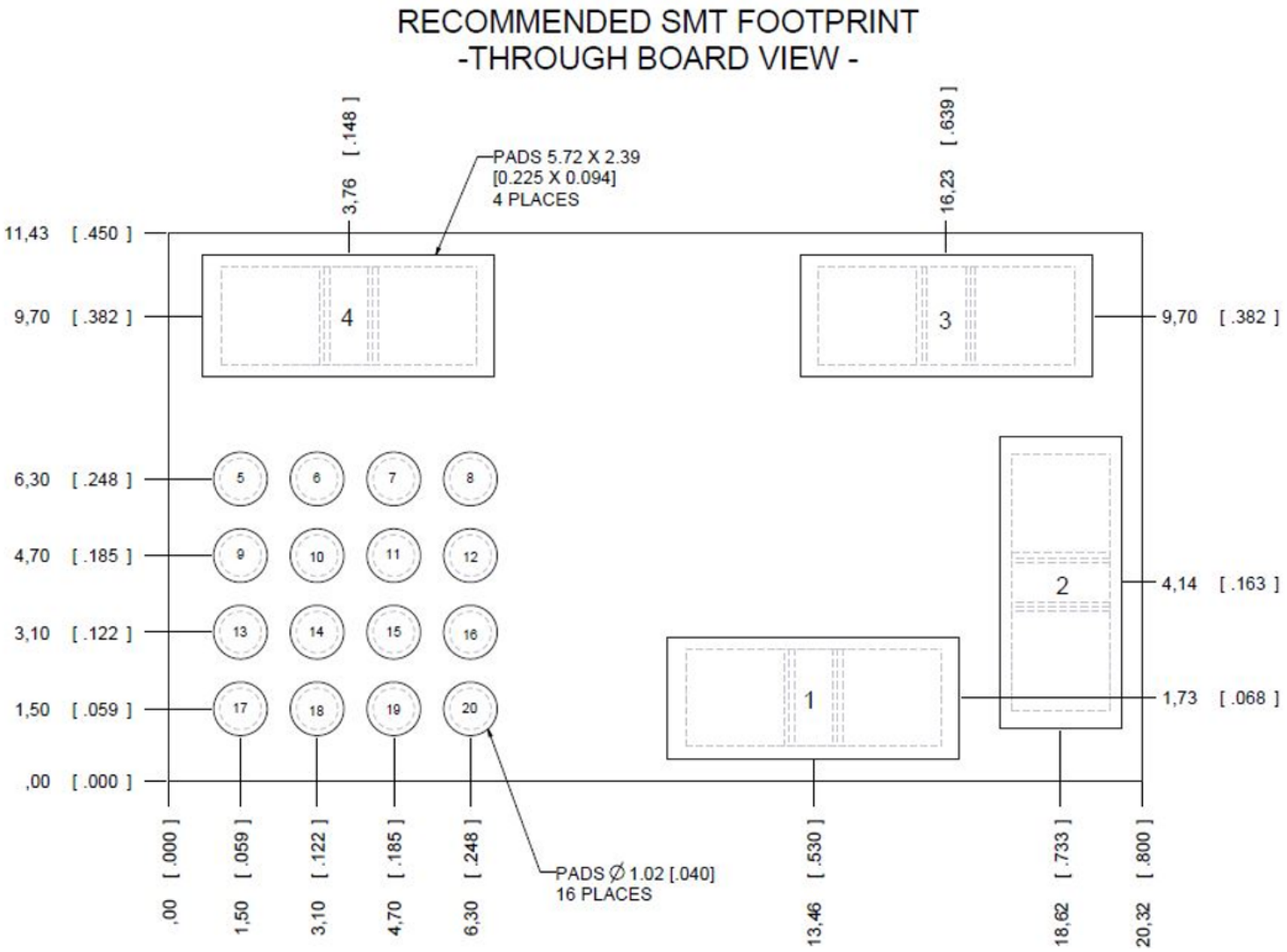

Figure 38. Footprint dimensions

Pin Assignment Table

Pin	Label	Type	Description
1	VIN	PWR	Input voltage rail. Connect the input filter capacitors between pins 1 and 2. See layout recommendation section for details. Minimum recommended capacitance 1 x 470µF (electrolytic) || 5 x 22 µF || 2 x 0.1µF.
2	GND	PWR	Input rail return.
3	GND	PWR	Output rail return.
4	VOUT	PWR	Output voltage rail. Connect the output filter capacitors between pins 4 and 3. See layout recommendation section for details. Minimum recommended capacitance 2 x 330µF (polymer) || 12 x 47 µF || 4 x 0.1µF.
5	SEQ	I	Output tracking voltage input. Reference the tracking source to pin 10. If not used, connect to SIG_GND.
6	VS-	I	Differential remote sense input. Connect to negative output regulation point.
7	VS+	I	Differential remote sense input. Connect to positive output regulation point.
8	V5P	O	Auxiliary 5V low power (5mA max) bus. Does not need external filter capacitors.
9	VSET	Multi	Used to set the POL address and the output voltage. See address table for details. Connect to the middle point of the resistor divider between V1P5 and SIG_GND.
10	SIG_GND	SGND	Analog signal ground return.
11	V1P5	O	Auxiliary 1.5V low power bus. Do not connect any external load except VSET resistor divider. Does not require external filtering. See layout recommendations.
12	PG	O	Power-good output. Configured as open-drain by default. Require weak 10k pull-up to V5P. Could be re-configured as push-pull via PMBus.
13	DATA	I/O	Serial data. Connect to external host and/or to other devices. Requires a pull-up resistor to a 3.3V or 5.5V source. V5 source recommended.
14	SMBALERT#	O	Serial alert. Connect to external host if desired. Requires a pull-up resistor to a 3.3V or 5.5V source. V5 source recommended. If not used, this pin should be left floating.
15	GND	DGND	Digital signal ground return.
16	ON/OFF	I	Enable input. Active signal enables device. Recommended to be tied low during device configuration. The ON/OFF signal must be glitch free to achieved specified delay timing. Positive or negative pulse widths shorter than 10µs will be ignored.
17	CLK	I/O	Serial clock. Connect to external host and/or to other modules. Requires a pull-up resistor to a 3.3V or 5.5V source. V5 source recommended.
18	SYNC	I/O	Clock synchronization input. Used to sync to an external clock or to output the internal clock. When used as part of a SYNC bus in order to achieve phase spreading or as part of a current sharing rail, one of the devices must have this pin configured as an output, with no pull-up or pull-down resistors on the bus.
19	DDC	I/O	Single-wire current sharing and inter-device communication bus. Requires a pull-up resistor to a 3.3V or 5.5V source. V5 source recommended. Pull-up voltage must be present when the device is powered.
20	SHARE	I/O	Current sharing communication bus. Connect to other current share enabled modules to achieve droop-less current sharing. If not used, this pin should be left floating.

Packaging Details

The UJT060 Open Frame modules are supplied in tape & reel as standard. Modules are shipped in quantities of 110 modules per reel. All Dimensions are in millimeters and (in inches).

Pick and Place Location

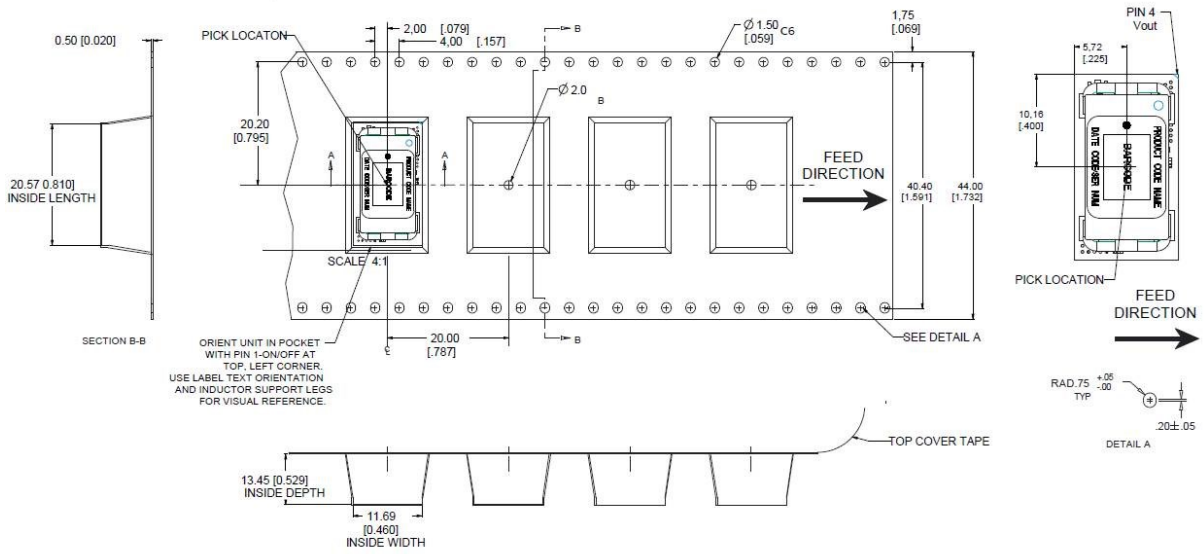

Figure 39. Pick and place location and Reel Dimensions

Reel Dimensions:

Outside Dimensions: 330.2 mm (13.00”)
Inside Dimensions: 177.8 mm (7.00”)
Tape Width: 44.00 mm (1.732”)

Packaging Details

Surface Mount Information

Pick and Place

The UJT060 Open Frame modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300 ℃. The label also carries product information such as product code, serial number and the location of manufacture.

Nozzle Recommendations

Stencil thickness of 7 mils minimum must be used for this product. The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7 mm.

Bottom Side / First Side Assembly

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Lead Free Soldering

The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

Pb-free Reflow Profile

Power Systems will comply with J-STD-020 Rev. D (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended linear reflow profile using Sn/Ag/Cu solder is shown in Fig. 40. Soldering outside of the recommended profile requires testing to verify results and performance.

Packaging Details

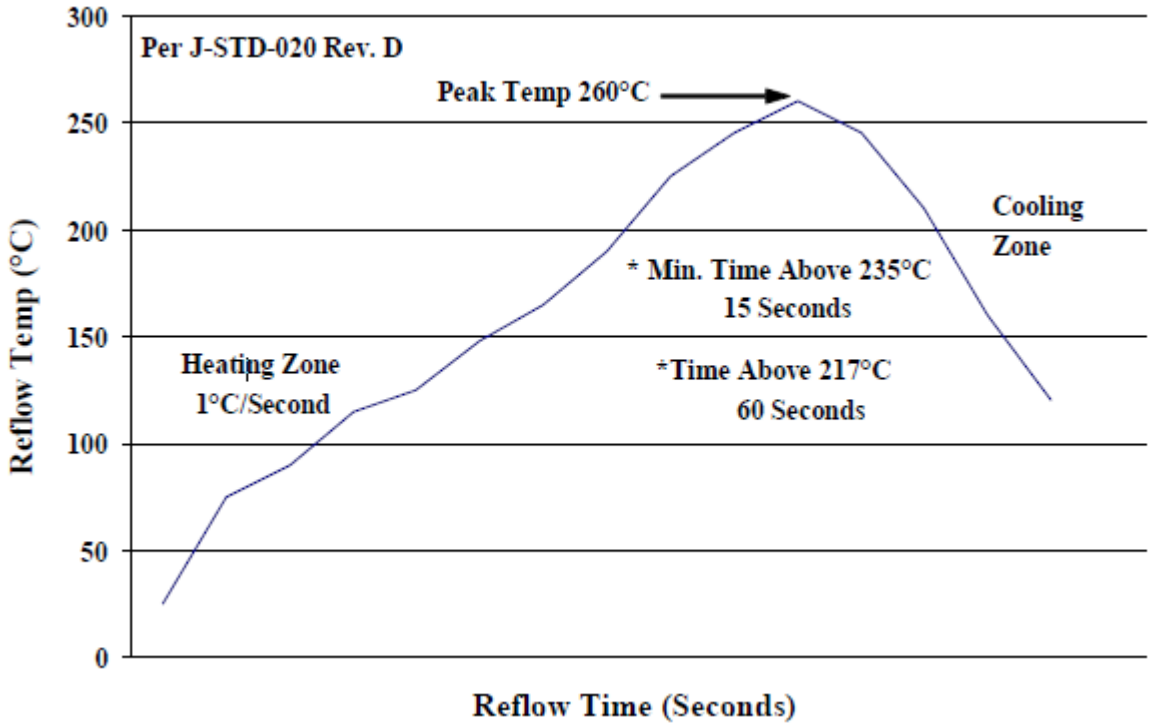

Figure 40. Recommended linear reflow profile using Sn/Ag/Cu solder

MSL Rating

The UJT060 Open Frame modules have a MSL rating of 2a.

Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of 30°C and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40° C, < 90% relative humidity.

Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to *Board Mounted Power Modules: Soldering and Cleaning* Application Note (AN04-001).

Change History (excludes grammar & clarifications)

Version	Date	Description of the change
1.1	2/5/2021	Initial Release
1.2/1.3	5/10/2021	Updated VOUT_UV_FAULT_LIMIT
1.4	5/14/2021	Updated Timescale Fig.10,16,22,28
1.5./1.6	5/24/2021	Updated PMBus table
1.7	6/14/2021	Updated 1.8V efficiency curve

Ordering Information

Please contact your ABB Sales Representative for pricing, availability and optional features.

Device Codes

Product Codes	Input Voltage	Output Voltage	Output Current	MSL Rating	Comcode
UJT060A0X43-SRPZ	7.5-14.4Vdc	0.5-2Vdc	60A	2a	1600157177A

Coding Scheme

Package Identifier	Family	Sequencing Option	Output current	Output voltage	On/Off logic	Remote Sense	Options		ROHS Compli-ance
U	J	T	60A0	X	4	3	-SR	-P	Z
P=Pico U=Micro D=Deca M=Mega G=Giga T=Tera	J = DLynx II Digital	T=with EZ Sequence X=without sequencing	60A	X = pro-gramm able output	4 = positive No entry = negative	3 = Remote Sense	S = Surface Mount R = Tape & Reel No entry = Through hole	Paralleling Pins	Z = ROHS6

ABB Power Electronics Inc.'s digital non-isolated DC-DC products may be covered by one or more of the following patents licensed from Bel Power Solution, Inc.: US20040246754, US2004090219A1, US2004093533A1, US2004123164A1, US2004123167A1, US2004178780A1, US2004179382A1, US20050200344, US20050223252, US2005289373A1, US20060061214, US2006015616A1, US20060174145, US20070226526, US20070234095, US20070240000, US20080052551, US20080072080, US20080186006, US6741099, US6788036, US6936999, US6949916, US7000125, US7049798, US7068021, US7080265, US7249267, US7266709, US7315156, US7372682, US7373527, US7394445, US7456617, US7459892, US7493504, US7526660.
Outside the US BEL Power Solutions, Inc. licensed technology is protected by patents: AU3287379AA, AU3287437AA, AU3290643AA, AU3291357AA, CN10371856C, CN1045261OC, CN10458656C, CN10459360C, CN10465848C, CN11069332A, CN11124619A, CN11346682A, CN1685299A, CN1685459A, CN1685582A, CN1685583A, CN1698023A, CN1802619A, EP1561156A1, EP1561268A2, EP1576710A1, EP1576711A1, EP1604254A4, EP1604264A4, EP1714369A2, EP1745536A4, EP1769382A4, EP1899789A2, EP1984801A2, W004044718A1, W004045042A3, W004045042C1, W004062061 A1, W004062062A1, W004070780A3, W004084390A3, W004084391A3, W005079227A3, W005081771A3, W006019569A3, W02007001584A3, W02007094935A3

ABB
601 Shiloh Rd.
Plano, TX USA

Go.ABB/Industrial