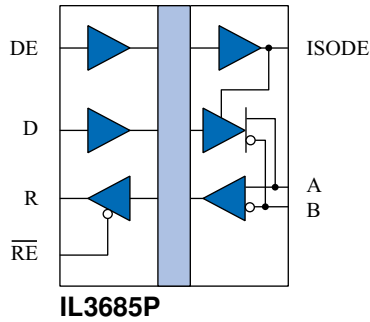


High-Speed Isolated 3.3 V Bus RS-485 Transceiver

Functional Diagrams



$V_{ID} (A-B)$	DE	\overline{RE}	R	D	Mode
$\geq 200 \text{ mV}$	L	L	H	X	Receive
$\leq -200 \text{ mV}$	L	L	L	X	Receive
$\geq 1.5 \text{ V}$	H	L	H	H	Drive
$\leq -1.5 \text{ V}$	H	L	L	L	Drive
X	X	H	Z	X	Hi-Z R
Open	L	L	H	X	Receive

Features

- 3.3 V bus
- Up to 40 Mbps data rate
- 1/5 unit load (supports up to 160 nodes)
- 20 ns propagation delay
- 5 ns pulse skew
- 50 kV/ μs typ.; 30 kV/ μs min. common mode transient immunity
- 44000 year barrier life
- 16.5 kV bus ESD protection
- Low EMC footprint
- Thermal shutdown protection
- $-40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$ temperature range
- Meets or exceeds ANSI RS-485 and ISO 8482:1987(E)
- 600 V_{RMS} working voltage
- 2500 V_{RMS} isolation voltage
- VDE V 0884-11 certified and UL 1577 approved
- 0.3" True 8™ mm 16-pin SOIC package

Applications

- DC-DC convertor-powered busses
- Factory automation
- Industrial control networks
- Building environmental controls

Description

IL3685-Series galvanically isolated, high-speed differential bus transceivers are designed for bidirectional data communication on balanced transmission lines. The devices use NVE's patented* IsoLoop spintronic Giant Magnetoresistance (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The IL3685P delivers at least 1.5 V into a 54 Ω load for excellent data integrity over long cable lengths. The device is compatible with 3.3 V RS-485 busses and 3.3 V or 5 V controller interfaces.

Current limiting and thermal shutdown features protect against output short circuits and bus contention that may cause excessive power dissipation. Receiver inputs feature a "fail-safe if open" design, ensuring a logic high R-output if A/B are floating.

Absolute Maximum Ratings⁽⁷⁾

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	-55		150	°C	
Junction Temperature	T_J	-55		150	°C	
Voltage Range at A or B Bus Pins		-7		12	V	
Supply Voltage ⁽¹⁾	V_{DD1}, V_{DD2}	-0.5		7	V	
Digital Input Voltage		-0.5		$V_{DD} + 0.5$	V	
Digital Output Voltage		-0.5		$V_{DD} + 1$	V	
ESD (bus nodes)		16.5			kV	Air gap Discharge per IEC61000-4-2

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltages	V_{DD1} V_{DD2}	3 3		5.5 3.6	V	
Ambient Operating Temperature	T_A	-40		85	°C	
Junction Temperature	T_J	-40		100	°C	
High-Level Digital Input Voltage	V_{IH}	2.4 3.0		V_{DD1}	V	$V_{DD1} = 3.3\text{ V}$ $V_{DD1} = 5.0\text{ V}$
Low-Level Digital Input Voltage	V_{IL}	0		0.8	V	
Differential Input Voltage ⁽²⁾	V_{ID}			+12 / -7	V	
High-Level Output Current (Driver)	I_{OH}			60	mA	
High-Level Digital Output Current (Receiver)	I_{OH}			8	mA	
Low-Level Output Current (Driver)	I_{OL}	-60			mA	
Low-Level Digital Output Current (Receiver)	I_{OL}	-8			mA	
Digital Input Signal Rise and Fall Times	t_{IR}, t_{IF}					DC Stable

Insulation Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)		8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)		0.013	0.016		mm	
Barrier Resistance	R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance	C_{IO}		7		pF	f = 1 MHz
Leakage Current			0.2		μA_{RMS}	240 V_{RMS} , 60 Hz
Comparative Tracking Index	CTI	≥ 600			V_{RMS}	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	1000			V_{RMS}	At maximum operating temperature
	DC	1500			V_{DC}	
Surge Immunity ("V" Version)	V_{IOSM}	12.8			kV _{PK}	Per IEC 61000-4-5
Barrier Life			44000		Years	100°C, 1000 V_{RMS} , 60% CL activation energy

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	θ_{JA}		67		°C/W	Double-sided PCB in free air
Junction–Case (Top) Thermal Resistance	θ_{JC}		12			
Junction–Ambient Thermal Resistance	θ_{JA}		46			
Junction–Case (Top) Thermal Resistance	θ_{JC}		9			
Power Dissipation	P_D			1.5	W	2s2p PCB in free air per JESD51

Safety and Approvals

VDE V 0884-11 / IEC 60747-17 (Basic Isolation; VDE File Number 5016933-4880-0001)

- Isolation voltage (V_{ISO}): 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000 V_{PK}
- Surge rating: 4000 V_{PK}
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit.
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit.
- Working Voltage (V_{IORM} ; pollution degree 2): 400 V_{RMS}

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	$^{\circ}C$
Safety rating power (180 $^{\circ}C$)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

UL 1577 (Component Recognition Program File Number E207481)

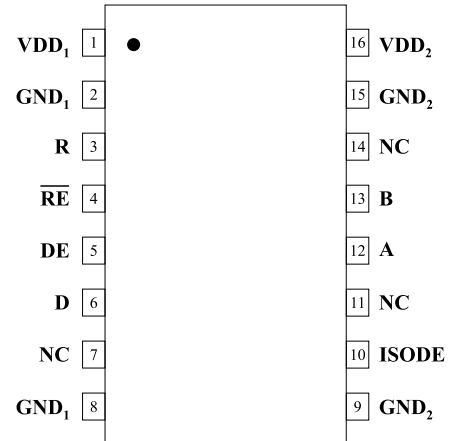
- 2500 V rating.
- Each part tested at 3000 V_{RMS} (4243 V_{PK}) for 1 second.
- Each lot sample tested at 2500 V_{RMS} (3536 V_{PK}) for 1 minute.

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

Pin Connections

1	V _{DD1}	Input power supply.
2	GND ₁	Input power supply ground return (pin 2 is internally connected to pin 8).
3	R	Output data from bus.
4	$\overline{\text{RE}}$	Read data enable (if $\overline{\text{RE}}$ is high, R= high impedance).
5	DE	Drive enable.
6	D	Data input to bus.
7	NC	No internal connection.
8	GND ₁	Input power supply ground return (pin 8 is internally connected to pin 2).
9	GND ₂	Output power supply ground return (pin 9 is internally connected to pin 15).
10	ISODE	Isolated DE output for use in PROFIBUS applications where the state of the isolated drive enable node needs to be monitored.
11	NC	No internal connection.
12	A	Non-inverting bus line.
13	B	Inverting bus line.
14	NC	No internal connection.
15	GND ₂	Output power supply ground return (pin 15 is internally connected to pin 9).
16	V _{DD2}	Output power supply.



Driver Section

Electrical Specifications (T_{min} to T_{max} and $V_{DD} = 3\text{ V}$ to 3.6 V unless otherwise stated)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Output voltage	V_O			V_{DD}	V	$I_O = 0$
Differential Output Voltage ⁽²⁾	$ V_{OD1} $			V_{DD}	V	$I_O = 0$
Differential Output Voltage ⁽²⁾	$ V_{OD2} $	1.5	2.1	3.5	V	$R_L = 54\ \Omega$
Differential Output Voltage ⁽²⁾	V_{OD3}	1.5	2.1	3.5	V	$R_L = 60\ \Omega$; $-7\text{ V} < V_{CM} < 12\text{ V}$
Change in Magnitude of Differential Output Voltage ⁽⁴⁾	$\Delta V_{OD} $			± 0.2	V	$R_L = 54\ \Omega$ or $100\ \Omega$
Common Mode Output Voltage	V_{OC}			3	V	$R_L = 54\ \Omega$ or $100\ \Omega$
Change in Magnitude of Common Mode Output Voltage ⁽⁴⁾	$\Delta V_{OC} $			± 0.2	V	$R_L = 54\ \Omega$ or $100\ \Omega$
High Level Input Current	I_{IH}			10	μA	$V_I = 3.5\text{ V}$
Low Level Input Current	I_{IL}			-10	μA	$V_I = 0.4\text{ V}$
Absolute Short-circuit Output Current	I_{OS}			250	mA	$-7\text{ V} < V_O < 12\text{ V}$

Receiver Section

Electrical Specifications (T_{min} to T_{max} and $V_{DD2} = 3.0$ V to 3.6 V unless otherwise stated)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Positive-going Input Threshold Voltage	V_{IT+}			0.2	V	-7 V < V_{CM} < 12 V
Negative-going Input Threshold Voltage	V_{IT-}	-0.2			V	-7 V < V_{CM} < 12 V
Hysteresis Voltage ($V_{IT+} - V_{IT-}$)	V_{HYS}		28		mV	$V_{CM} = 0$ V, $T = 25^{\circ}$ C
Differential Bus Input Capacitance	C_D		9	12	pF	
High Level Digital Output Voltage	V_{OH}	$V_{DD} - 0.2$	V_{DD}		V	$V_{ID} = 200$ mV $I_{OH} = -20$ μ A
Low Level Digital Output Voltage	V_{OL}			0.2	V	$V_{ID} = -200$ mV $I_{OH} = 20$ μ A
High-impedance-state output current	I_{OZ}			± 1	μ A	$V_O = 0.4$ to $(V_{DD2} - 0.5)$ V
Line Input Current	I_I			220	μ A	$V_I = 12$ V
				-160	μ A	$V_I = -7$ V
Input Resistance	R_I	60			k Ω	

Switching Characteristics

$V_{DD1} = 5$ V, $V_{DD2} = 3.3$ V						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Data Rate		40			Mbps	$R_L = 54$ Ω , $C_L = 50$ pF
Propagation Delay ⁽⁵⁾	t_{PD}		20	30	ns	$V_O = -1.5$ to 1.5 V, $C_L = 15$ pF
Pulse Skew ⁽⁶⁾	$t_{SK}(P)$		1	5	ns	$V_O = -1.5$ to 1.5 V, $C_L = 15$ pF
Skew Limit ⁽³⁾	$t_{SK}(LIM)$		2	10	ns	$R_L = 54$ Ω , $C_L = 50$ pF
Output Enable Time To High Level	t_{PZH}		15	30	ns	$C_L = 15$ pF
Output Enable Time To Low Level	t_{PZL}		15	30	ns	$C_L = 15$ pF
Output Disable Time From High Level	t_{PHZ}		15	30	ns	$C_L = 15$ pF
Output Disable Time From Low Level	t_{PLZ}		15	30	ns	$C_L = 15$ pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	$ CM_H , CM_L $	30	50		kV/ μ s	$V_{CM} = 1500$ V _{DC} $t_{TRANSIENT} = 25$ ns
$V_{DD1} = 3.3$ V, $V_{DD2} = 3.3$ V						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Data Rate		40			Mbps	$R_L = 54$ Ω , $C_L = 50$ pF
Propagation Delay ⁽⁵⁾	t_{PD}		25	35	ns	$V_O = -1.5$ to 1.5 V, $C_L = 15$ pF
Pulse Skew ⁽⁶⁾	$t_{SK}(P)$		2	5	ns	$V_O = -1.5$ to 1.5 V, $C_L = 15$ pF
Skew Limit ⁽³⁾	$t_{SK}(LIM)$		4	10	ns	$R_L = 54$ Ω , $C_L = 50$ pF
Output Enable Time To High Level	t_{PZH}		17	30	ns	$C_L = 15$ pF
Output Enable Time To Low Level	t_{PZL}		17	30	ns	$C_L = 15$ pF
Output Disable Time From High Level	t_{PHZ}		17	30	ns	$C_L = 15$ pF
Output Disable Time From Low Level	t_{PLZ}		17	30	ns	$C_L = 15$ pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	$ CM_H , CM_L $	30	50		kV/ μ s	$V_{CM} = 1500$ V _{DC} $t_{TRANSIENT} = 25$ ns

Power Consumption

T _{min} to T _{max} and V _{DD2} = 3.0 V to 3.45 V unless otherwise stated							
Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Controller-Side Quiescent Supply Current	V _{DD1} = 3.3 V V _{DD1} = 5 V	I _{DD1}		1 2	2 6	mA	f _{IN} = 0 Hz
Bus-Side Quiescent Supply Current		I _{DD2}		4	6	mA	R _T = ∞; Outputs Enabled; f _{IN} = 0 Hz
Controller-Side Dynamic Supply Current		I _{DD1}		0.18		mA/Mbps	V _{DD1} = 3.3 V
Bus-Side Dynamic Supply Current		ΔI _{DD2} /Δf _{IN}		0.75 0.55			R _T = ∞ R _T = 60 Ω
Transceiver Power Dissipation		I _{DD1} × V _{DD1} + I _{DD2} × V _{DD2}		17 150		mW	R _T = ∞; f _{IN} = 0 Hz R _T = 60 Ω; f _{IN} = 40 Mbps; excludes R _T power dissipation

Magnetic Field Immunity⁽⁸⁾

V _{DD1} = 5 V, V _{DD2} = 5 V							
Power Frequency Magnetic Immunity		H _{PF}		3500		A/m	50 Hz / 60Hz
Pulse Magnetic Field Immunity		H _{PM}		4500		A/m	t _p = 8 μs
Damped Oscillatory Magnetic Field		H _{OSC}		4500		A/m	0.1 Hz – 1 MHz
Cross-axis Immunity Multiplier ⁽⁹⁾		K _X		2.5			
V _{DD1} = 3.3 V, V _{DD2} = 5 V							
Power Frequency Magnetic Immunity		H _{PF}		1500		A/m	50 Hz/ 60 Hz
Pulse Magnetic Field Immunity		H _{PM}		2000		A/m	t _p = 8 μs
Damped Oscillatory Magnetic Field		H _{OSC}		2000		A/m	0.1 Hz – 1 MHz
Cross-axis Immunity Multiplier ⁽⁹⁾		K _X		2.5			

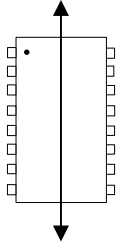
Notes:

- All voltages are with respect to network ground except differential I/O bus voltages.
- Differential input/output voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
- Skew limit is the maximum propagation delay difference between any two devices at 25°C.
- Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
- Includes 10 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
- Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel.
- Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
- The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 8.
- External magnetic field immunity is improved by this factor if the field direction is “end-to-end” rather than to “pin-to-pin” (see diagram on p. 8).

Electromagnetic Compatibility

IL3685-Series Transceivers are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is “end-to-end” (rather than to “pin-to-pin”) as shown in the diagram at right:



Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Power Supply Decoupling

V_{DD1} and V_{DD2} should be bypassed with 100 nF ceramic capacitors as close as possible to V_{DD} pins.

DC Correctness

The IL3685 incorporates a patented refresh circuit to maintain the correct output state with respect to data input. At power up, the bus outputs will follow the Function Table shown on Page 1. The DE input should be held low during power-up to eliminate false drive data pulses from the bus. An external power supply monitor to minimize glitches caused by slow power-up and power-down transients is not required.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Typical Performance Graphs

The following graphs show typical performance (25 °C; $V_{DD1} = V_{DD2} = 3.3\text{ V}$ unless otherwise stated):

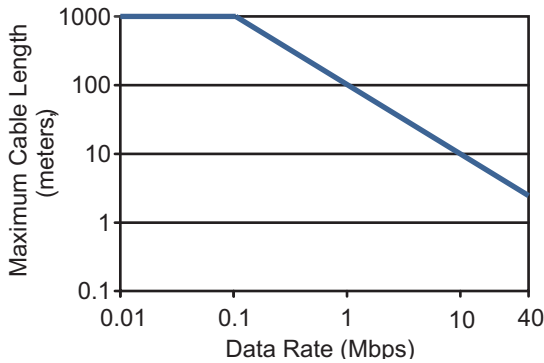


Figure 1. Maximum cable length versus data rate.

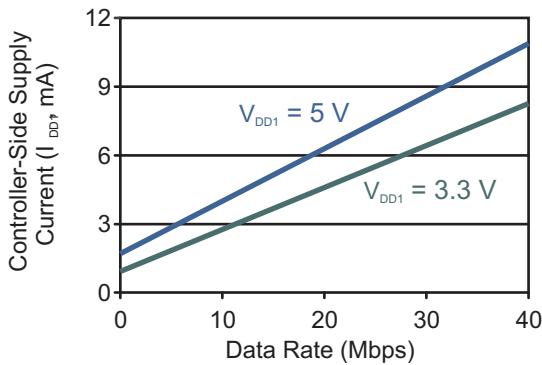


Figure 2. Typical controller-side supply current (I_{DD2}) versus data rate.

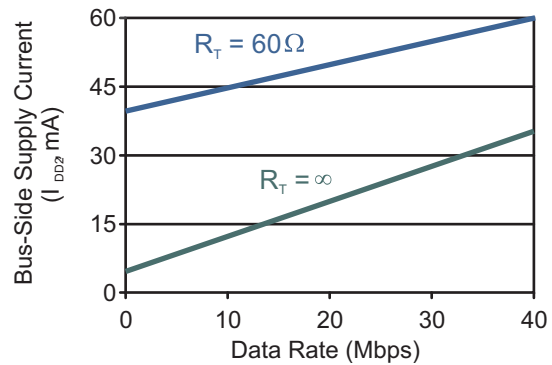


Figure 3. Typical bus-side supply current (I_{DD2}) versus data rate.

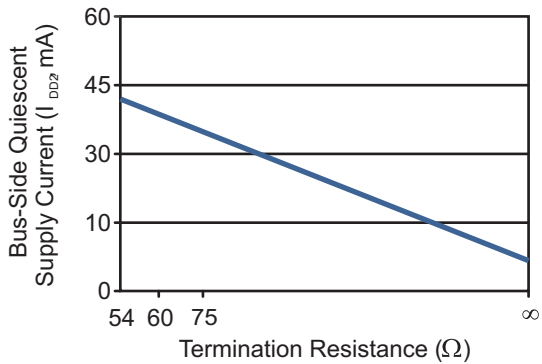


Figure 4. Typical bus-side supply current (I_{DD2}) versus aggregate termination resistance.

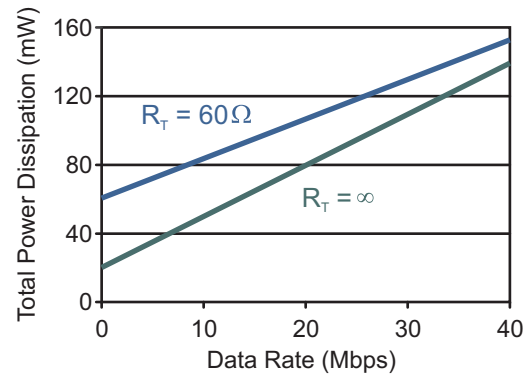


Figure 5. Typical transceiver power dissipation versus data rate (excludes R_T power dissipation).

Application Information

Receiver Features

The receiver output “R” has tri-state capability via the active low \overline{RE} input.

Driver Features

Drivers feature low propagation delay skew to maximize bit width and minimize EMI. Drivers have tri-state capability via the active-high DE input.

Receiver Data Rate, Cables and Terminations

Shielded twisted pair bus cable is recommended for high transmission speeds (more than 500 Kbps). IL3685-Series transceivers are intended for networks up to 1,000 meters shielded twisted pair proper termination. The maximum data rate decreases as cable length increases. Unshielded or untwisted can be at used at low baud rates and short distances.

Typical Application

The following schematic shows a typical isolated RS-485 bus power supply and node:

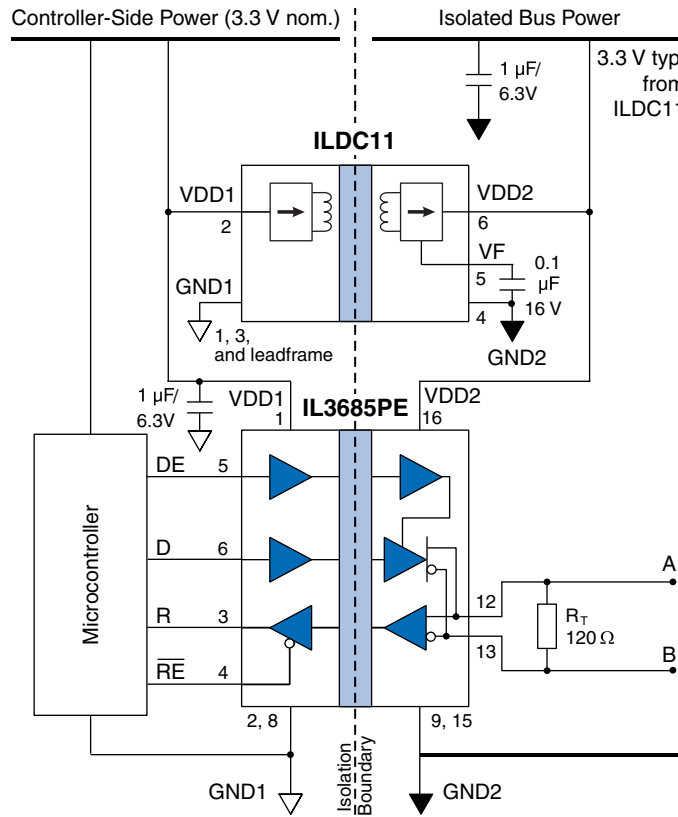
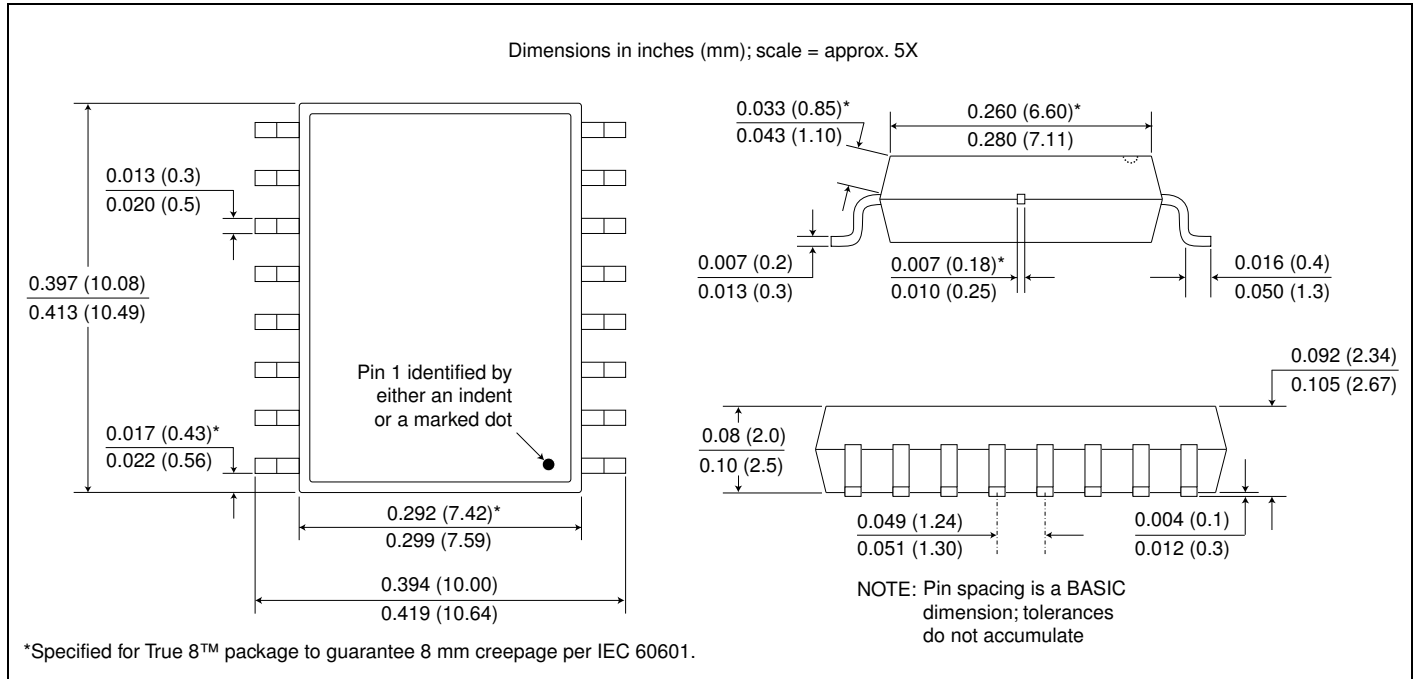
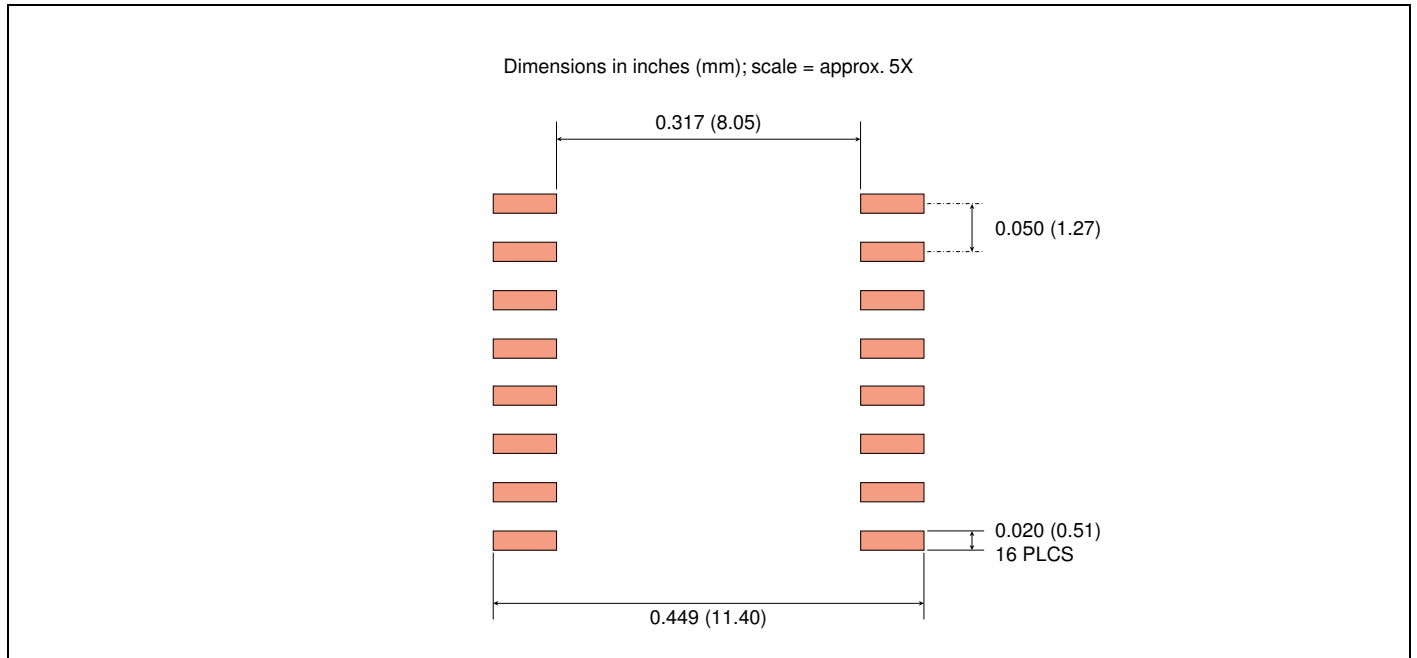


Figure 6. Typical circuit for isolated RS-485 bus supply and node.

Package Drawing

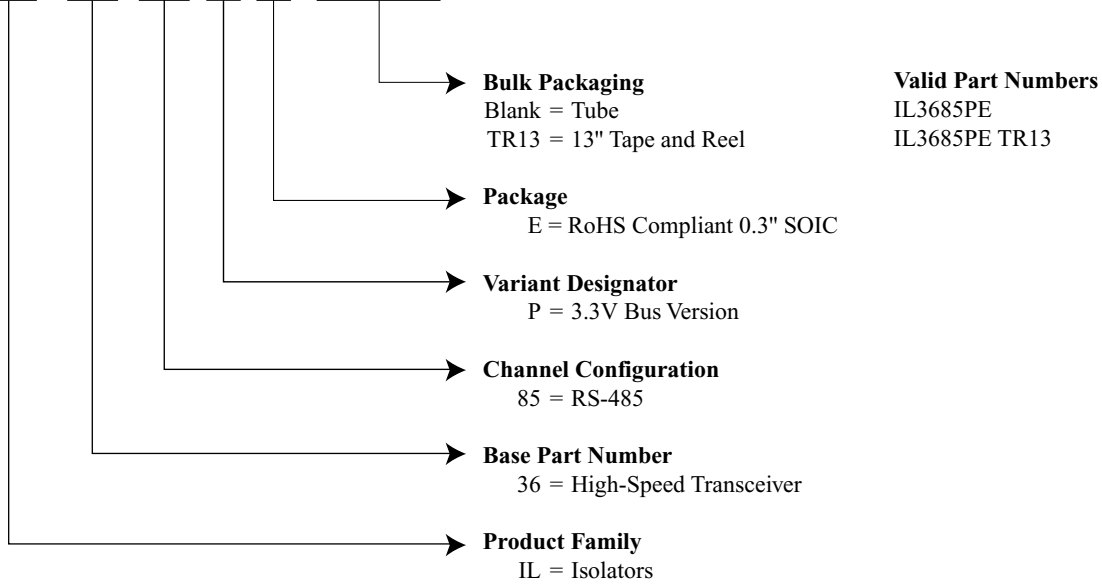


Recommended Pad Layout



Ordering Information and Valid Part Numbers

IL 36 85 P E TR13



Revision History

ISB-DS-001-IL3685P-D
January 2020

Change

- Updated VDE certification to VDE V 0884-11.
- Deleted PROFIBUS logo since the IL3685P is typically PROFIBUS compliant but not guaranteed.
- Updated EMC specifications (p. 8).
- Added maximum cable length versus data rate Typical Performance Graph (p. 9).
- Added DC-DC convertor reference design (p. 11).
- Misc. minor changes.

ISB-DS-001-IL3685P-C
December 2019

Change

- Broke out power consumption specifications in separate table; tightened specs (p. 7).
- Added typical performance charts for power vs. speed (p. 8).

ISB-DS-001-IL3685P-B
November 2019

Changes

- Corrected Recommended Operating Conditions—Supply Voltage— V_{DD2} (p. 2).
- Updated Thermal Characteristics (p. 2).
- Cosmetic changes and rewrites (p. 7).

ISB-DS-001-IL3685P-A
December 2017

Changes

- Revised thermal specifications.
- Initial release.

ISB-DS-001-IL3685P-PRELIM
May 2017

Change

- Preliminary release.

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ISB-DS-001-IL3685P-D

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