Using Microchip's Micropower LDOs

Author: *Paul Paglia,*
Microchip Technology Inc.

INTRODUCTION

Microchip Technology, Inc.'s family of micropower LDOs utilizes low-voltage CMOS process technology. These LDOs provide similar ripple rejection and drop-out characteristics as their bipolar equivalents, but are significantly more efficient. A typical bipolar regulator has base current equal to 1-2% of the output load, whereas Microchip's LDOs have approximately 60 µA resulting in total operating current orders of magnitude lower than their bipolar counterparts. In addition, Microchip's LDOs can be placed in a shutdown mode, further enhancing their effectiveness in low-power applications.

This low-power operation makes Microchip's family of LDOs ideal for upgrading the LP2980 and MIC5205 bipolar LDOs in cellular phones, pagers, PDAs, laptops, hand-held meters, and other portable applications.

Microchip's micropower LDOs are available with fixed and adjustable outputs, supporting load currents up to 50 mA, 100 mA, 150 mA and 300 mA. SOT-23-5, SOT-23-6, SOT-223, and MSOP-8 packaging require minimal board space. Shutdown capability, thermal protection, and current limiting are standard in every device. Adjustable output, error flag, and noise bypass capability are provided on select devices (see Table 3).

APPLICATIONS

Optimizing Output Voltage Accuracy of TC1070/TC1071 Adjustable LDOs

Microchip's LDOs are available in both adjustable and fixed output voltage options. The accuracy of the output depends on the initial accuracy, stability, and temperature coefficient of the internal bandgap reference and the feedback resistors.

Rather than specifying V_{OUT} accuracy on adjustable regulators, the initial accuracy and temperature coefficient of the internal reference is specified. V_{OUT} accuracy is not specified because it depends on the external feedback resistors. Figure 1 shows a typical adjustable LDO feedback circuit in which resistors R_1 and R_2 set the output voltage per the following formula:

EQUATION 1:

$$V_{OUT} = V_{REF}[(R_1/R_2) + 1]$$

V_{REF} = 1.20V

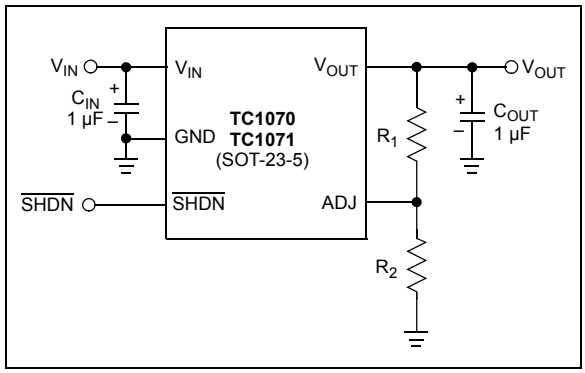

FIGURE 1: *Adjustable LDO Feedback Circuit.*

The ADJ pin is a high impedance CMOS input. Consequently, resistor values can be between 300 kΩ and 1 MΩ to minimize the current through R_1 and R_2.

Inspection of Equation 1 reveals the following:

1. When V_{OUT} is made equal to V_{REF} (i.e., R_1 is zero), the tolerance of V_{OUT} will be approximately that of V_{REF}.
2. The tolerance of V_{OUT} is a function of both the tolerance of V_{REF} and the tolerance of the R_1/R_2 ratio when V_{OUT} is greater than V_{REF} (i.e., when $R_1/R_2 > 0$).

For the purposes of worst case analysis, the tolerances of R_1 and R_2 are additive. For example, if R_1 and R_2 are both 1% resistors, the maximum tolerance of the R_1/R_2 ratio is 2%.

Re-examining the effect of tolerances on Equation 1 reveals that the tolerance of V_{OUT} worsens proportionally as the V_{OUT} setting departs the value of V_{REF}. Stated another way:

EQUATION 2:

$$ERROR_{VOUT} \alpha (V_{OUT} - V_{REF})$$

Table 1 shows that percentage of total output voltage error contributed by the tolerances of V_{REF} and R_1/R_2 for various values of V_{OUT}.

TABLE 1: OUTPUT ERROR CONTRIBUTORS

V_{OUT} (V)	Reference Tolerance (%)	Resistor Tolerance (%)	Resistor Error (%)	Total Output Error (%)
1.23	2	1	0	2
1.23	2	2	0	2
2.0	2	1	0.77	2.77
2.0	2	2	1.54	3.54
2.46	2	1	1.0	3.0
2.46	2	2	2.0	4.0
3.0	2	1	1.2	3.2
3.0	2	2	2.4	4.2
4.0	2	1	1.38	3.38
4.0	2	2	2.76	4.76
5.0	2	1	1.50	3.5
5.0	2	2	3.0	5.0

The output voltage accuracy of the adjustable regulator improves with tighter tolerance resistors. However, accuracy will be limited to ±2% due to the accuracy of the reference. Table 2 shows output voltage accuracy for the adjustable LDO using 1%, 0.5%, and 0.1% tolerance resistors.

TABLE 2: RESISTOR TOLERANCE EFFECT ON V_{OUT} ERROR

V_{OUT}	V_{OUT} Error		
	1% Resistor Tol.	0.5% Resistor Tol.	0.1% Resistor Tol.
5.0V	3.5%	2.75%	2.15%
4.0V	3.38%	2.69%	2.14%
3.0V	3.2%	2.6%	2.12%
2.46V	3.0%	2.5%	2.10%
2.0V	2.77%	2.39%	2.08%
1.23V	2.0%	2.0%	2.0%

Power-Saving Shutdown Mode

All of Microchip's micropower LDOs have a shutdown input that allows the user to digitally disconnect the load from the power source and send the regulator into a low-power "sleep" mode. The supply current is reduced from 50 µA, during normal operation, to 0.05 µA in shutdown.

The $\overline{SHDN}$ pin input current is guaranteed to be no greater than 1 µA (an order of magnitude lower than bipolar counterparts).

Shutdown mode is activated when $\overline{SHDN}$ is below 0.2 x V_{IN}. In this mode, the pass transistor is turned OFF, disconnecting the load from the power source.

Shutdown mode is disabled, allowing normal device operation, when the input is above 0.4 x V_{IN}. This V_{IN} is low enough to ensure that a control output from a 3.3V microcontroller, operating from four fully-charged NiCad/NiMH cells (6V), can enable the LDO. If not used, $\overline{SHDN}$ should not be left floating, but rather connected to V_{IN}.

Out-of-Regulation (ERROR) Flag

The TC1070/1/2/3 and TC1054/5 each have Error Flag outputs that are asserted when the LDO falls out of regulation by approximately –5%.

The $\overline{ERROR}$ pin is an N-channel open-drain output that can sink up to 1 mA. However, larger value pull-up resistors should be selected so that energy loss through $\overline{ERROR}$ is kept to a minimum. ERROR must be pulled to any supply voltage less than 7V through a pull-up resistor.

$\overline{ERROR}$ output is valid for input voltages above 1V and undefined for voltages below 1V. As the output is transitioning between 0V and 1.0V during power up/down, the Error output may float momentarily to 1.0V. If 1.0V is high enough to be interpreted as a logic '1', the two-resistor network shown in Figure 2 may be used.This will ensure that $\overline{ERROR}$ never will rise above 0.5V during invalid states. Keep in mind the maximum that Error output can bein its high state is $V_{OUT}/2$.

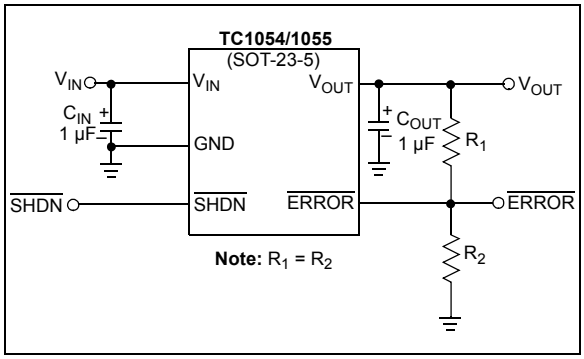

FIGURE 2: *Ensuring Valid Error Output for Low V_{IN} Levels.*

By connecting an RC on $\overline{\text{ERROR}}$ output, it can be used as a power on reset. During power up, the Error comparator will go high as soon as the regulator output is within tolerance. $\overline{\text{ERROR}}$ will be delayed by the RC network before releasing the microcontroller from reset.

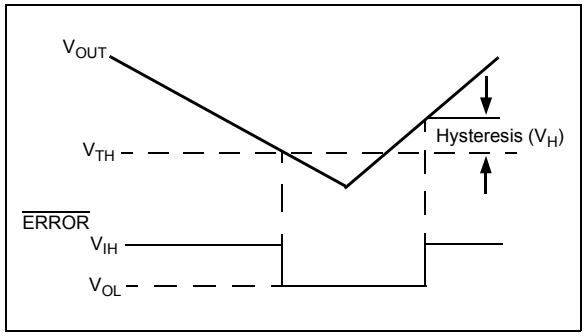

FIGURE 3: *Out-of-Regulation Error Flag.*

$\overline{\text{ERROR}}$ also can be used as a power quality monitor. If a low input voltage or an over-current condition causes the output to fall out of regulation, $\overline{\text{ERROR}}$ will pull low, signifying an unstable power condition. This flags the microcontroller, which now can activate proper shutdown sequencing, ensuring orderly system operation.

The Error comparator has 50 mV of positive hysteresis to provide some V_{IN} noise immunity.

Input, Output and Bypass Capacitors

It is recommended that input, output, and bypass capacitors be used for optimal device performance. To ensure stability in the LDO's feedback loop, a capacitor is required from the output to ground (Figures 4 and 5). Capacitors must be chosen that meet the ESR value range and minimum capacitance identified in device data sheets. In general, a 1 µF - 2.2 µF capacitor is recommended to ensure stable operation under maximum load conditions. Larger value capacitors (4.7 µF to 10 µF) will increase transient load response and ripple rejection performance.

Ceramic capacitors offer the lowest ESR followed by, in order of increasing ESR, OS-CON, film, aluminum electrolytic, and tantalum. Film capacitors provide good performance, but usually are not a viable solution due to excessive cost and size. Ceramics combine excellent ESR with relatively small size. However, the ESR of ceramic capacitors sometimes can be too low, requiring a 1Ω series resistor to ensure stability. OS-CON capacitors offer an ESR only slightly higher than ceramics, but consume more volume. The OS-CON capacitors exhibit rock-solid ESR from –55°C to 125°C. Aluminum electrolytics are ideal for low-cost commercial temperature grade applications where board space is not a concern. Like OS-CON capacitors, electrolytics typically are offered in a radial lead package, but are available in surface mount styles. Tantalums offer an ESR similar to aluminum electrolytics. They also provide a reasonable cost, high-volume efficiency solution and are usually the capacitor of choice.

A 1 µF input capacitor should be installed from V_{CC} to GND (Figures 4 and 5) if the IC is powered from a battery or if there is excessive (>1 ft) distance between the regulator and the AC filter capacitor. A larger value capacitor will provide better V_{CC} noise rejection and improved performance when the supply has a high AC impedance. A 470 pf bypass capacitor can be tied to the bypass pin on the TC1014/1015 and TC1072/1073 or the ADJ pin on the TC1070/1071 (see Figure 5) to reduce the V_{REF} noise.

Thermal Issues

The amount of power that the LDO dissipates is a function of the bias supply current and the pass-through current. The pass-through current is the current that flows from V_{CC} through the pass transistor of the LDO to the load. The following equation is used to calculate power dissipation:

EQUATION 3:

$$P_D = (V_{CC} \times I_S) + [(V_{CC} - V_{OUT})I_{LOAD}]$$

Maximum values of V_{CC} and I_{LOAD} and minimum values for V_{OUT} should be used when calculating P_D to ensure worst-case conditions are met.

The amount of power that the LDO can dissipate depends on the ambient temperature (T_A). A guard-banded maximum die temperature (T_{JMAX}) of +125°C is used to account for variations in thermal conductivity of PC boards and variations in airflow.

EQUATION 4:

$$\theta_{JA} = (T_{JMAX} - T_A)/PD_{MAX}$$
$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

θ_{JC} is the thermal resistance from the die surface to the package body and leads. θ_{CA} is the thermal resistance from the package body and leads to the surrounding air, PC board dielectric, and traces.

The SOT-23-5 and SOT-23-6 packages have a worst-case θ_{JA} of 220°C/W when mounted on a single-layer FR4 dielectric copper-clad PC board. This θ_{JA} can be reduced by using a PC board made with a dielectric that has a better heat transfer coefficient. Additionally, adding a ground plane and large supply traces to the IC will provide better thermal conductivity. The values for θ_{JA} are for a system that uses natural convection. A significant reduction in θ_{CA} can be induced with forced airflow.

Given:

θ_{JA} = 220°C/W

$\therefore PD_{MAX} = (125°C - T_A)/220°C/W$

Ambient Temperature	P_{DMAX}
+25°C	0.454W
+50°C	0.341W
+85°C	0.182W

Excessive power dissipation will result in elevated die temperatures that could activate the device's thermal shutdown. The LDOs have an integrated thermal protection circuitry that disables the LDO when die temperatures exceed approximately +160°C. Ten degrees Celsius of hysteresis is built into the protection circuitry, such that the LDO is not released from thermal shutdown until the die temperature drops to +150°C. In addition to thermal protection, an internal sense resistor in series with the pass element providesa short-circuit limit.

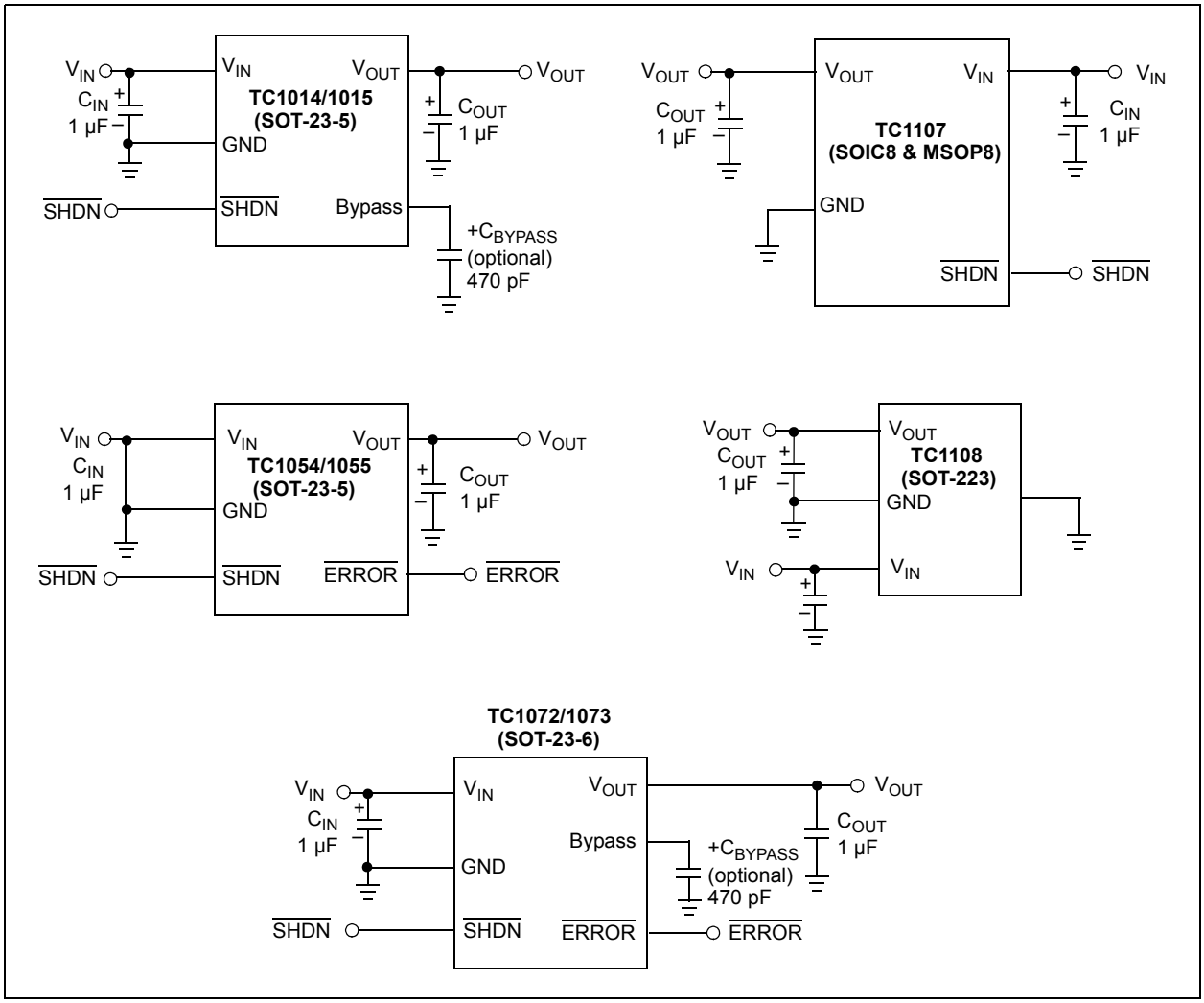

FIGURE 4: *Typical Application Circuit (Fixed Output)*

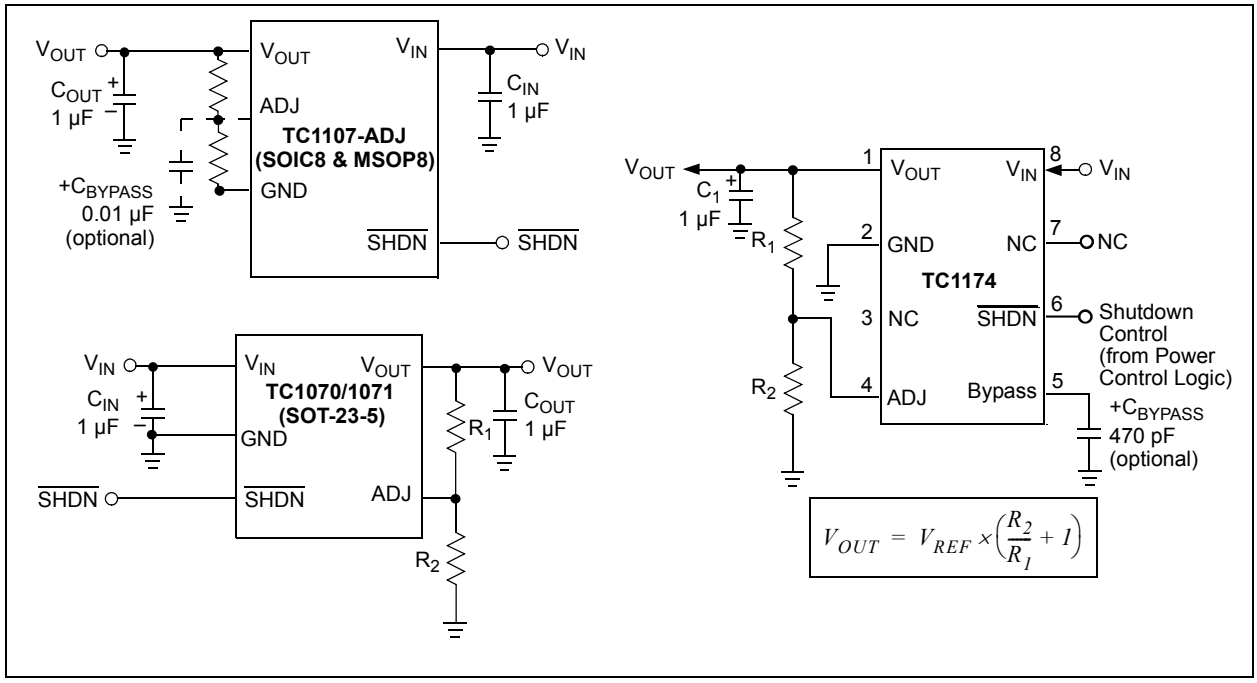

FIGURE 5: *Typical Application Circuit (Adjustable Output).*

TABLE 3: CMOS LDOS SELECTION GUIDE

Part No.	Package	Output Voltage †											ADJ	SHDN	Error Flag	Bypass	I_{SS} Typ. (µA)	I_{OUT} Max (mA)	V_{DROP} Typ. (mV)
		2.5V	2.7V	2.8V	2.84V	2.85V	3.0V	3.15V	3.3V	3.6V	4.0V	5.0V							
TC1014	SOT-23-5	X	X			X	X		X	X	X	X		X		X	50	50	85
TC1015	SOT-23-5	X	X			X	X		X	X	X	X		X		X	50	100	180
TC1054	SOT-23-5	X	X			X	X		X	X	X	X		X	X		50	50	85
TC1055	SOT-23-5	X	X			X	X		X	X		X		X	X		50	100	180
TC1070	SOT-23-5												X	X			50	50	85
TC1071	SOT-23-5												X	X			50	100	180
TC1072	SOT-23-6	X	X			X	X		X	X	X	X		X		X	50	50	85
TC1073	SOT-23-6	X	X			X	X		X	X	X	X		X		X	50	100	180
TC1107	MSOP-8, SOIC-8			X			X		X			X		X		X	50	300	240
TC1108	SOT-223			X			X		X			X					50	300	240
TC1173	MSOP-8, SOIC-8			X			X		X			X		X	X	X	50	100	180
TC1174	MSOP-8, SOIC-8												X	X		X	50	300	240
TC1185	SOT-23-5	X	X			X	X		X	X	X	X		X		X	50	150	270
TC1186	SOT-23-5	X	X			X	X		X	X	X	X		X	X		50	150	270
TC1187	SOT-23-5												X	X	X		50	150	270
TC1188*	SOT-23-5			X	X			X						X			50	100	55
TC1189*	SOT-23-5			X	X			X						X			50	100	55
TC1223	SOT-23-5	X	X			X	X		X	X	X	X		X			50	50	85
TC1224	SOT-23-5	X	X			X	X		X	X	X	X		X			50	100	180

* Pin Compatible Replacement for MAX8863/8864.

† Custom Output Voltages Available - Contact Microchip Technology.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona, Gresham, Oregon and Mountain View, California. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Habour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Fuzhou
Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde
Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7250
Fax: 86-29-8833-7256

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Gumi
Tel: 82-54-473-4301
Fax: 82-54-473-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Penang
Tel: 60-4-646-8870
Fax: 60-4-646-5086

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

12/08/06