An Analysis for Power Dissipation of LDO Application with High Power

When an LDO is operating, its on-chip devices dissipate power as a heat way. Heat flow from a higher to a lower temperature region. For LDO regulator, most of the dissipated power comes from the power or pass transistor of IC. Therefore, the current passes through the power transistor and the voltage across the transistor, which determine the amount of heat generated. The quantity that resists or impedes this flow of heat energy is called thermal resistance.

Introduction:

The paper provides user to know the thermal dissipation of LDO regulators, how to select a heat sink and prevent thermal problem from exceeding maximum allowable junction temperature. For LDO regulators, the thermal resistance data of different packages are compliant with different applications and user's requirements, as well as determine the thermal limits of different packages as in the spec. Thermal resistance, such as $R\theta_{JA}$ and $R\theta_{JC}$, are applied to determine thermal dissipation performance for LDO regulator. A low thermal resistance represents better performance than a high thermal resistance. A system that has a lower thermal resistance can either dissipate more heat for a given temperature difference or dissipate a given amount of heat with a smaller temperature difference.

Thermal topology of LDO:

As shown in figure 1, the thermal resistance is the resistance from the package to heat dissipation and is the reciprocal of thermal conductivity of the package. The source of heat is the chip in the package. All materials in the heat flow path between the IC and the outside environment have thermal resistance and the temperature of the chip rises above ambient environment. Therefore, the thermal conductivity of the silicon chip, molding compound, copper of leadframe, and the thickness and thermal conductivity of die adhesion material all affect the rate at which the heat is dissipated. As figure1, the thermal resistance $R\theta_{JP}$ and $R\theta_{PA}$ can be neglected because most of the heat flows through the case and into the surrounding air. Same as an electrical resistance, summing these series resistance determines the value of $R\theta_{JA}$ (the chip junction to ambient thermal resistance).

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CS} + R\theta_{SA}$$

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$$

for heat sink of PCB issue

$R\theta_{JC}$ = thermal resistance from junction to case

$R\theta_{CS}$ = thermal resistance from case to heat sink

$R\theta_{SA}$ = thermal resistance from heat sink to ambient

$R\theta_{CA}$ = thermal resistance from case to ambient

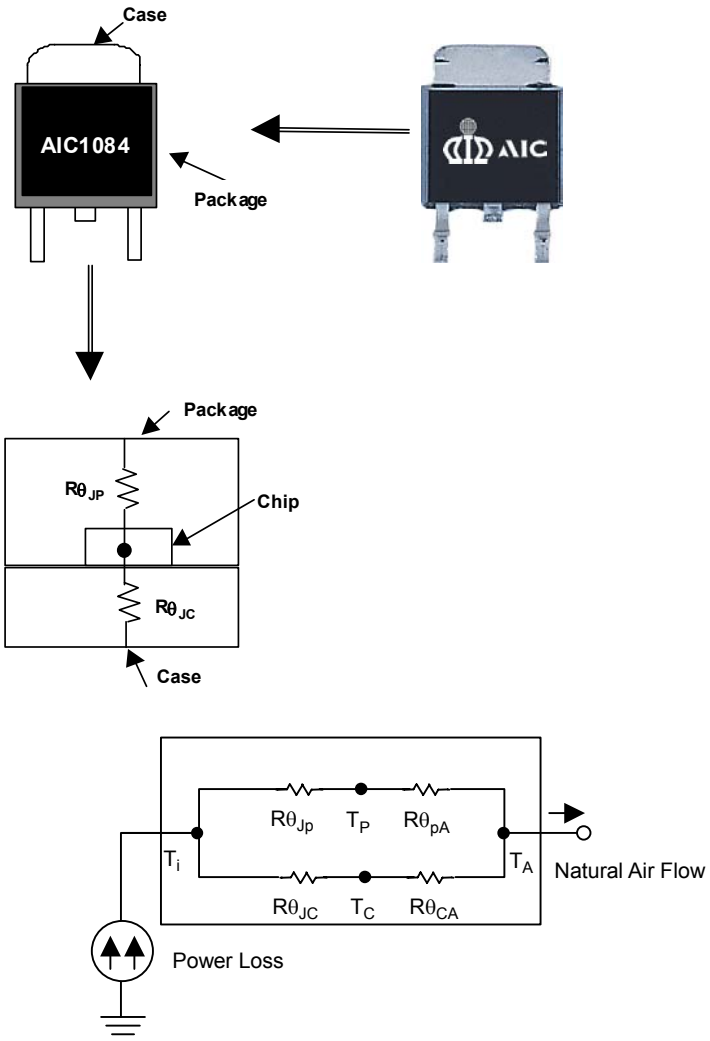


Figure1: AIC1084 Package Thermal Metrics

Fundamental formula for thermal resistance $R\theta_{JA}$ and $R\theta_{JC}$:

The heat on the die flows through the case, package and into the surrounding air. And it must be removed at a sufficient rate to keep the temperature of the transistor junction in the regulator from damage. When the heat quantity generated by a device is equal to that removed, the condition of a steady state is achieved. Therefore, most of the silicon manufacturers follow the junction temperature, $T_{J(max)}$, which is 125°C. T_A, the ambient temperature, is usually between -20°C and 80°C. And $T_{J(max)}$ and T_A are both specified in the IC spec of the LDO. The maximum power dissipation of an IC package is depended on $R\theta_{JA}$ and $R\theta_{JC}$, which are a measure of relative performance of the IC. When $R\theta_{JA}$ and $R\theta_{JC}$ are out of the allowing range in the LDO spec, neither the heat of IC can be removed nor the junction temperature be maintained below 125°C.

When the external heat sinks are applied, $R\theta_{JA}$ decreases with $R\theta_{JC}$ remaining the same.

The thermal resistance $R\theta_{JA}$ and $R\theta_{JC}$ are defined as:

$$R\theta_{JA} = \frac{T_J(max) - T_A}{P_D(max)}$$

$$R\theta_{JC} = \frac{T_J(max) - T_C(max)}{P_D(max)}$$

where:

T_J =maximum recommended junction temperature

T_A =ambient temperature of user environment

T_C =maximum case temperature

$R\theta_{JA}$ =junction to ambient thermal resistance of LDO

P_D =maximum recommended power dissipation

How to select and calculate correct SOA for high power LDO:

Safe operating area (SOA) of LDO maintains IC junction temperature below the maximum allowable temperature under normal operating environment. To select an SOA to achieve normal junction temperature of LDO, users need to employ the following four fundamental steps.

- The amount of heat P_D being generated by the IC for power limit
- The maximum allowable junction temperature T_J can be available from data book of AIC
- The maximum ambient temperature T_A
- The thermal resistance $R\theta_{JC}$ can be available from databook of AIC
- Selected correct safe operating area for maximum power dissipation application
- Selected maximum power limit for user requirement

Step1: For example: V_{IN} =5V, V_{OUT} =3.3V, I_{OUT} =1A, $R\theta_{JC}$ =6°C/W (TO-263), T_A =25°C how to choose safe operating area =?mm^2 and I_{OUT} (max)=?A for user maximum power dissipation.

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} = (5 - 3.3) \times 1 = 1.7W$

1.7W is user operating PD.

Step2: Find the value of the thermal resistance you need ($R\theta_{JA}$) for 115mm^2 and the value of the maximum power limit (P_D max).

That is, the thermal resistance $R\theta_{JA}$ is 54.5°C/W with power limit P_D (max) at 1.83W when the heat sink of 115mm^2 pattern is required. So, in the case, the power dissipation P_D =1.7W shall be below power limit P_D (max) when the loading current is 1A.

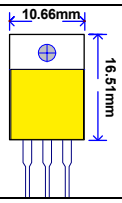
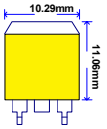
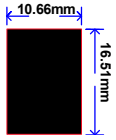
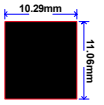
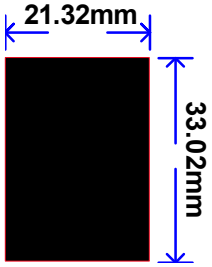
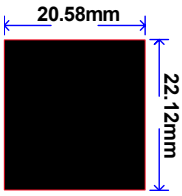
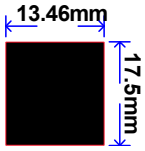
Step3: Continuing the above example, the AIC1084CM junction temperature T_J can be obtained as follows:

$$R\theta_{JA} = \frac{T_J(max) - T_A}{P_D} = \frac{T_J - 25}{1.7} = 54.5\,^{\circ}C/W$$

$$\Rightarrow T_J = 117.65^{\circ}C \quad \langle\langle \quad 125^{\circ}C$$

We can find that the system is stable in terms of heat when P_D (max)<<1.83W, thermal resistance (junction to ambient) $R\theta_{JA}$=54.5°C/W<< 60°C/W and safe operating area are chosen suitably. In addition, the thermal resistance $R\theta_{JA}$ for TO-263 surface-mount package is 60°C/W (no heatsink) as defined in AIC data book. We need a heat sink when we would like to decrease thermal resistance of surface-mount package to $R\theta_{JA}$=54.5°C/W (which is less than 60°C/W as said in AIC data book).

Table1: top view of the thermal test pattern for AIC1084 in actual scale

CT TO-220		CM TO-263		CE TO-252	
Copper area, 1oz, 175mm^2		Copper area, 1oz, 115mm^2		Copper area, 1oz, 60mm^2	
Copper area, 1oz, 700mm^2		Copper area, 1oz, 460mm^2		Copper area, 1oz, 240mm^2	

Conclusion

Until now, the heat problem of high power LDO is perplexing to choose appropriates heatsink (PCB) for the device and the lower thermal resistance. Even, the price of LDO is another consideration for the user to employ the application of LDO. According to the above calculation of thermal resistance and junction temperature, we have found that the thermal resistance affects dissipative heat of the system. It is an important factor that the thermal resistance $R\theta_{JA}$ and $R\theta_{JC}$ influence the rate of heat dissipation when the maximum input voltage, maximum load current, highest ambient operating temperature,and nominal output voltage, based on the spec, are applied. In addtion, we also must follow the maximum power dissipation (power limit) and maximum junction to ambient thermal resistance requirements. If the selected pakage can't meet the requirement of thermal resistance limits, we will need a heat sink to keep IC junction temperaure below 125°C. Therefore, for high power of LDO series products with all kinds of power dissipation, it is essential to add or choose enough area of heatsink.

Besides, LDO thermal shutdown, a protective function, is triggered when an LDO is abnormally operated in a high environment or power dissipation, which are out of the limits of the spec. Thermal shutdown, at a temperature between 155 to 165°C, of LDO from AIC equips the system to protect from damage.

Reference:

- AIC1084 5A low dropout positive adjustable regulator from analog integrated corp.